

### Course Information

Lecture Meeting:	MW 7:00-8:20 PM
Lecture Room:	229 NH
Lecture Instructor:	Dr. Nader Hozhabri
Lab Meeting:	Fridays 9 AM - 12:50 PM
Lab Room:	NANO 104
Lab Instructor:	Dr. Samir Iqbal
Office Hours and Location:	Thursdays 12 PM to 1 PM in NANO 217
Lab Instructor Contact:	817.272.0228 / SMIQBAL@uta.edu
Lab GTA:	Mr. Waseem Asghar
LAB GTA Email:	waseem.asghar@mavs.uta.edu

**Course Description:** his course covers major sections of IC fabrication and process. Course comprises of lecture and lab.

**Text:** Silicon Processing for the VLSI Era  
Volume 1, 2<sup>nd</sup> Edition, Process Technology  
By: S. Wolf and R. N. Tauber

#### Lecture:

The areas to be covered in this course are

1- Semiconductors and Insulators: Definition, crystal structures, and their physical properties.

#### 2- Wafer Fabrication:

- a) Czochralski (CZ)
- b) Float Zone (FZ)
- c) Molecular Beam Epitaxy (MBE)

#### 3- Crystal defects:

Monovacancy, Divacancy, Microvoids, Voids, Antisites, Interstitials, Dislocation, Stacking fault, Grain Boundaries, Precipitates (clusters).

#### 4- Diffusion:

- a) Fick's first and second law and their solutions
- b) Mechanism of diffusion
- c) Profile and Junction Depth and techniques of their determination
- d) Effect of electric field on diffusion process
- e) Diffusion of most used impurities in IC fabrication (Boron, Phosphorus, Arsenic).
- f) Principals of SUPREM process simulation
- g) Diffusion Systems [equipments, Sources (gas, liquid, solid)]
- h) Measurement techniques.

#### 5- Thermal Oxidation (SiO<sub>2</sub>) and Nitridation

- a) Structure and physical properties
- b) Oxidation Kinetic (general solution, Parabolic and linear growth and empirical modifications to the growth rate of SiO<sub>2</sub> and its kinetic).
- c) Thermal Nitridation
- d) Factors which affect oxidation rate

EE5343 -- Silicon Integrated Circuit Fabrication Technology  
Fall 2009

- e) Applications of Oxide and Nitride layers in IC fabrication.
- f) SiO<sub>2</sub>/Si interface and charge traps and impurities redistribution at the interface.
- g) Oxidation systems.
- h) Measurement techniques.

**6- Ion Implantation:**

- a) Dose, Beam Current, Range and Projected Range.
- b) Projected and Lateral Straggle
- c) Ion Stopping (nuclear and electronic energy loss mechanism)
- d) Implantation in amorphous and single crystal (channeling effect)
- e) Ion implantation damage.
- f) Electrical activation and implantation damage recovery (Annealing and RTP)
- g) Ion Implantation Equipments
- h) Masking layers
- i) Shallow Junction
- j) Measurement Techniques

**7- Photolithography**

- a) Photolithography steps (Coat, Soft bake, Patterning and Exposure (Step), Post Exposure Bake, Develop, Inspection)
- b) Photo resists (positive and negative)
- c) Resist chemistry (Photo sensitive and base)
- d) Physical properties (Sensitivity, Photo Speed, Resolution, etc..)
- e) Coat and Coaters (Thickness control, uniformity , ...)
- f) Soft Bake and its effects on the film properties and consequent steps
- g) Patterning and exposure, Criteria, limits, resist dependency, equipments, alignment, etc.)
- h) Bosung Curves, Focus-exposure matrix, ...
- i) Post Exposure Bake, and its effects on the pattern
- j) Develop (batch, spray, and puddle) Develop chemistry, develop time,
- k) Critical Dimensions (CD) and Inspection (pattern integrity, notching, bridging, etc.)

**8- Interconnect**

- a) Metal (Al, Ti, TiN, W, etc..)
- b) CVD and PVD techniques and systems,
- c) Al, Al:Si, Al:Si:Cu in VLSI (properties, alloys, etc..)
- d) Sputter Deposition for VLSI (glow discharge, rf sputter, magnetron sputter, mechanism, deposition rate, advantages and disadvantages, etc.)
- e) Contacts and Vias
- f) Morphology and Step Coverage, Aspect Ratio
- g) Refractory Metals, and application
- h) Barrier metals
- i) Ohmic and Schottky contacts
- j) Silicide formation
- k) Effects of contamination (water, carbon, etc..)
- l) Planarization and Passivation

**9- Etch**

- a) Etch type (wet, dry)
- b) Dry Etch (Plasma etch (Process, mechanism, its chemistry and physics)
- c) Reactive Ion Etching (Process, mechanism, its chemistry and physics, damage etc.)
- d) Wet Etching (chemical and chemistry, etch rate, application and process, etc.)

EE5343 -- Silicon Integrated Circuit Fabrication Technology  
Fall 2009

- 10- Process Integration and Device Fabrication (all steps)
- 11- Runcard (Trailer)
- 12- Clean Room
- 13- Statistical Process Control, charts, limits, determination of limits, etc..

**Lab:**

- Practical part of this course will be done in Nanotechnology Research and Teaching Facility (NanoFAB).
- In the practical part of the course, the basics of each step of the process will be practiced. This include (oxidation, metalization, photolithography, etch)
- Fab will be held Fridays 9 am to 12:50 pm.
- Also students will use the available facilities to construct a Capacitor with different oxide films (one oxide film will be processed at the UTA facility and two types will be provided to them from NSC) as their project. All Capacitors will be tested.

**Grading, Homework, Exams, Project and their criteria:**

Homework: 10 %  
Term paper: 10 %  
Project and lab work: 25 %  
Midterm: 25 %  
Final: 30 %

All exams will be closed books

**Attendance Policy:** The course content will evolve around class-discussions and laboratory fabrication. It would be imperative to attend the lecture and lab to grasp the concepts and follow the material. If you can not present/deliver the work assigned to you, provide one week advance notice to the instructors. Be prepared to present documentation supporting the absence.

**Make-up Exam/Assignment Policy:** If you can not meet an assignment deadline or appear for an exam, give the instructors one-week advance notice. No credit will be given for the missed assignment/exam unless such absence/delay/failure-to-deliver occurs due to a documented emergency. You will be required to furnish written evidence to confirm the nature of emergency.

**Drop Policy:** The UT-Arlington drop policy will be followed as per the time table here:  
[http://www3.uta.edu/registrar/registration\\_schedule\\_Fall2009.asp](http://www3.uta.edu/registrar/registration_schedule_Fall2009.asp)

**Americans With Disabilities Act:** The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 92-112 - The Rehabilitation Act of 1973 as amended. With the passage of federal legislation entitled *Americans with Disabilities Act (ADA)*, pursuant to section 504 of the Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens.

The instructors are required by law to provide "reasonable accommodations" to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with informing faculty of their need for accommodation and in providing authorized documentation through designated administrative channels. Information regarding specific diagnostic criteria and policies for obtaining academic accommodations can be found at [www.uta.edu/disability](http://www.uta.edu/disability). Also, you may visit the Office for Students with Disabilities in room 102 of University Hall or call them at (817) 272-3364.

**Academic Integrity:** It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University. You are required to carefully read and sign the form titled "STATEMENT ON ETHICS, PROFESSIONALISM, AND CONDUCT FOR ENGINEERING STUDENTS." If you need soft copy of this statement, email the instructors/GTA.

"Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts." (Regents' Rules and Regulations, Series 50101, Section 2.2)

For the first occurrence of academic dishonesty by a student, a zero grade will be given on the exam, report, assignment, or project, as the case may be. Second occurrence of academic dishonesty by the same student (individual or in a team) will result in automatic reduction of one grade letter in the final grade of the course. The Office of Student Judicial Affairs will be informed in writing if two or more cases of academic dishonesty are found for any student.

Plagiarism has many shapes, but can be explained in a few examples under the scope of this course. It maybe presenting someone else's published words (and work) in a way that these words (and works) do not clearly show the source. Any text from someone else's work can not be used "verbatim" unless in double quotes and followed by a citation and appropriate credit. If in doubt, ask the instructors/GTA.

**Student Support Services Available:** The University of Texas at Arlington supports a variety of student success programs to help you connect with the University and achieve academic success. These programs include learning assistance, developmental education, advising and mentoring, admission and transition, and federally funded programs. Students requiring assistance academically, personally, or socially should contact the Office of Student Success Programs at 817-272-6107 for more information and appropriate referrals.

**E-Culture Policy:** The University of Texas at Arlington has adopted the University email address as an official means of communication with students. Through the use of email, UT-Arlington is able to provide students with relevant and timely information, designed to facilitate student success. In particular, important information concerning registration, financial aid, payment of bills, and graduation may be sent to students through email.

EE5343 -- Silicon Integrated Circuit Fabrication Technology  
Fall 2009

All students are assigned an email account and information about activating and using it is available at [www.uta.edu/email](http://www.uta.edu/email). New students (first semester at UT-Arlington) are able to activate their email account 24 hours after registering for courses. There is no additional charge to students for using this account, and it remains active as long as a student is enrolled at UT-Arlington. Students are responsible for checking their email regularly.

The instructors/GTA will send important course-related information to your UT-Arlington e-mail address ONLY. Your email to the instructor/GTA should also come from a UT-Arlington email account. Your email message sent from non-UT-Arlington accounts may never reach the instructor/GTA. You will be responsible for any misplaced or misdirected email that is sent from non-UT-Arlington email address.

**Grade Grievance Policy:** If you have any grievance regarding a grade, consult with the instructor/GTA. Information about the UT-Arlington grievance policy is here:  
[http://www.uta.edu/gradcatalog/general\\_info#grievances](http://www.uta.edu/gradcatalog/general_info#grievances)

**Final Review Week:** A period of five class days prior to the first day of final examinations will be designated as FINAL REVIEW WEEK. The purpose of this week is to allow UT-Arlington students sufficient time to prepare for final exams. During this week, there will be no schedule or required activities such as field trips, seminars, or performances; and no themes, research problems or exercises of similar scope that have a completion date during or following this week will be assigned unless specified in the class syllabus. During Final Review Week, no exams constituting 10% or more of the final grade will be given, except make-up tests and laboratory examinations. In addition, no portion of the final exam will be given during Final Review Week.