

### Course Information

Lecture Time and Room: Tuesdays and Thursdays 5:30-6:50 PM in NH 108  
Lab Meeting and Room: Mondays and Wednesdays 12:00-3:50 PM in NANO 104

**Instructor** Contact: Dr. Samir Iqbal (SMIQBAL@uta.edu / 817.272.0228)  
O/Hs and Location: Mondays and Wednesdays 4-5 PM in NANO 217

**Lecture GTA** Info: Mr. Waseem Asghar (waseem.asghar@mavs.uta.edu)  
Lecture GTA O/Hs: Wednesday 1:00-5:00 PM in NanoFab students' cubicle

**Lab GTA** Info: Mr. Azhar Ilyas (azhar.ilyas@mavs.uta.edu)  
Lab GTA O/Hs: Thursday 1:30-3:30 PM in NanoFab students' cubicle

**Text:** Silicon Processing for the VLSI Era, Volume 1 - Process Technology, Second Edition,  
By: S. Wolf and R. N. Tauber. ISBN: 0-9616721-4-5. <http://www.latticepress.com/vol1page2.html>

**Course Description and Content:** Course comprises of lectures and lab. The course aims to provide an introduction to the basic fabrication steps and processes of integrated circuit semiconductor devices. Fundamental concepts of semiconductor physics will also be covered as follows:

- 1- Semiconductors and Insulators: Definition, crystal structures, physical properties.
- 2- Wafer Fabrication: Czochralski (CZ), Float Zone (FZ), Molecular Beam Epitaxy
- 3- Crystal Defects: Monovacancy, Divacancy, Microvoids, Voids, Antisites, Interstitials, Dislocation, Stacking fault, Grain Boundaries, Precipitates.
- 4- Diffusion:
  - a) Fick's first and second law and their solutions
  - b) Mechanism of diffusion
  - c) Profile and Junction Depth and techniques of their determination
  - d) Effect of electric field on diffusion process
  - e) Impurity diffusion in IC fabrication (Boron, Phosphorus, Ar).
  - f) Principles of SUPREM process simulation
  - g) Diffusion Systems [equipment, sources (gas, liquid, solid)]
  - h) Measurement techniques.
- 5- Thermal Oxidation and Nitridation of Silicon
  - a) Oxidation kinetics (general solution, Parabolic and linear growth and empirical modifications to the growth rate of  $\text{SiO}_2$  and its kinetics)
  - b) Thermal Nitridation
  - c) Factors in oxidation
  - d) Applications of oxide and nitride layers in IC fabrication.
  - e)  $\text{SiO}_2/\text{Si}$  interface, charge traps and impurities redistribution at the interface.
  - f) Oxidation systems.
  - g) Measurement techniques
- 6- Ion Implantation:

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- a) Dose, Beam Current, Range and Projected Range
- b) Projected and Lateral Straggle
- c) Ion Stopping (nuclear and electronic energy loss mechanism)
- d) Implantation in amorphous and single crystal (channeling effect)
- e) Ion implantation damage
- f) Electrical activation and implantation damage recovery (Annealing and RTP)
- g) Ion Implantation equipment
- h) Masking layers
- i) Shallow Junction
- j) Measurement techniques

**7-** Photolithography:

- a) Photolithography steps (Coat, Soft bake, Patterning and Exposure, Post Exposure Bake, Develop, Inspection)
- b) Photoresists (positive and negative)
- c) Resist chemistry (Photo sensitive and base)
- d) Physical properties (Sensitivity, Photo Speed, Resolution, etc.)
- e) Coat and Coaters (Thickness control, uniformity, etc.)
- f) Soft Bake and its effects on the film properties and consequent steps
- g) Patterning and exposure, Criteria, limits, resist dependency, equipment, alignment, etc.)
- h) Bosung Curves, Focus-exposure matrix
- i) Post Exposure Bake, and its effects on the pattern
- j) Develop (batch, spray, and puddle)
- k) Developer chemistry, develop time
- l) Critical Dimensions (CD) and Inspection (pattern integrity, notching, bridging, etc.)

**8-** Interconnects:

- a) Metal (Al, Ti, TiN, W, etc.)
- b) CVD and PVD techniques and systems,
- c) Al, Al:Si, Al:Si:Cu in VLSI (properties, alloys, etc.)
- d) Sputter Deposition for VLSI (glow discharge, RF sputter, magnetron sputter, mechanism, deposition rate, advantages and disadvantages, etc.)
- e) Contacts and Vias
- f) Morphology and Step Coverage, Aspect Ratio
- g) Refractory Metals and applications
- h) Barrier metals
- i) Ohmic and Schottky contacts
- j) Silicide formation
- k) Effects of contamination (water, carbon, etc.)
- l) Planarization and Passivation
- m) Chemical Mechanical Polishing

**9-** Etch:

- a) Etch type (wet, dry)
- b) Dry Etch, Plasma etch (Process, mechanism, its chemistry and physics)
- c) Reactive Ion Etching (Process, mechanism, characteristics. damage etc.)
- d) Wet Etching (chemical and chemistry, etch rate, application and process, etc.)

**10-** Process Integration and Device Fabrication (all steps)

**12-** Clean Room

**13-** Statistical Process Control, Charts, Limits, Determination of Limits, etc.

**Lab:**

- Lab work will be done in Nanotechnology Research and Teaching Facility (NanoFAB).

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- Every student has to pass the “NanoFAB Safety & Protocol Training” and “General HAZCOM Online Training.” The students who do not pass these trainings will be administratively dropped from the course.
- In the practical part of the course, the basics of each step of the process will be practiced. This includes oxidation, metallization, photolithography, etch, etc.
- Each student is assigned to a lab session for either Mondays or Wednesdays from 12 PM to 3:50 PM in NANO 104. Be in the lab on time.
- Lab sections can not be changed by the GTA/ instructor.
- Students will also use the available facilities to construct a capacitor with different oxide films (one oxide film will be processed at the UTA facility and two types will be provided to them from NSC) as their project. All capacitors will be tested.

**Evaluation/Grading Components of the Course:** The course requires several homework assignments, one term paper, properly maintained lab notebook and two exams. Wikipedia and/or other websites can not be used as a reference in any of the assignments of this course. Most of the assignments/projects are to be submitted through the WebCT course page. Name your file with your First and Last name followed by assignment name. For all assignments, present your original work. Each individual assignment has to be worked out by individual student. Look under “Academic Integrity” for further details.

The grade will be calculated as per the following breakdown:

Homework:	10%
Term paper:	25%
Project Lab Notebook:	30%
Midterm:	15%
Final:	20%

Term Paper: Towards the goals of developing a more interactive classroom environment and practicing analytical thinking and communication skills, each student has to write a term paper. The goal is to learn the process by which researchers, practicing engineers, and technology advisors, acquire, distill, process and present technically sound ideas based on alternative technological approaches to solve a problem. The aim is to turn data into meaningful information, and information into intelligence (actionable information).

The paper has to address a problem of semiconductor fabrication and processing. Breakdown the paper in three distinct sections. The introduction should describe and define the new idea on one page. Second part should provide a synopsis of impeding problems/limitations that are addressed and analysis of the state of the art. The third and most important part of the paper should present a technically sound detailed solution backed with theory, data or simulation. The term paper will be due on March 30, 2010 before class.

The first page of the paper will be shared with the rest of the class. Each student will be asked to give a 15 minute presentation on the term paper. The presentations will be scheduled from second week of April 2010. Everyone will be invited (and expected) to participate in the discussion. Your paper will account for the 15% of the overall grade while presentation will weigh 5% towards the overall grade.

The term paper should be normally on a topic not covered in the class. Restrict the paper to 10 pages (excluding cover page and references). Use Arial font size 11 or larger for every text in the paper. The margins on top, bottom, left and right of the page should not be less than 0.75 inch. Proper referencing should be done using IEEE format given at following web address:

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[www.ieee.org/portal/cms\\_docs\\_iportals/iportals/publications/pubservices/confpub/ieeecitationref.pdf](http://www.ieee.org/portal/cms_docs_iportals/iportals/publications/pubservices/confpub/ieeecitationref.pdf)

**Lab Notebooks:** The lab notebooks will be collected twice during the semester without prior announcement. The lab notebooks should have detailed records of all activities and experiments carried out in the lab under the headings of Purpose, Procedure, Equipment and Supplies, Precautions, Observations, Diagrams. The lab notebook should have numbered pages. Include details like data, data plots, data analysis, figures, sketches, diagrams, micrographs, pictures, etc. to support your observations.

**Exams:** All exams will be closed books. Midterm exam will be on Tuesday March 9, 2010 during class time in NH108. Final exam is tentatively scheduled for Tuesday May 11, 2010 at 5:30-8 PM. The date, time and room number for the final will be confirmed in April 2010.

**Attendance Policy:** The course content will evolve around class-discussions and laboratory fabrication. It would be imperative to attend the lecture and lab to grasp the concepts and follow the material. If you can not present/deliver the work assigned to you, provide one week advance notice to the instructor. Be prepared to present documentation supporting the absence.

**Make-up Exam/Assignment Policy:** If you can not meet an assignment deadline or appear for an exam, give the instructor one-week advance notice. No credit will be given for the missed assignment/exam unless such absence/delay/failure-to-deliver occurs due to a documented emergency. You will be required to furnish written evidence to confirm the nature of emergency.

**Drop Policy:** The UT-Arlington drop policy will be followed as per the time table here:  
[http://www3.uta.edu/registrar/registration\\_schedule\\_Spring2010\\_Regular.asp](http://www3.uta.edu/registrar/registration_schedule_Spring2010_Regular.asp)

**Americans with Disabilities Act:** The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 92-112 - The Rehabilitation Act of 1973 as amended. With the passage of federal legislation entitled *Americans with Disabilities Act (ADA)*, pursuant to section 504 of the Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens.

The instructor is required by law to provide "reasonable accommodations" to students with disabilities, so as not to discriminate on the basis of that disability. Students responsibility primarily rests with informing faculty of their need for accommodation and in providing authorized documentation through designated administrative channels. Information regarding specific diagnostic criteria and policies for obtaining academic accommodations can be found at [www.uta.edu/disability](http://www.uta.edu/disability). Also, you may visit the Office for Students with Disabilities in room 102 of University Hall or call them at (817) 272-3364.

**Academic Integrity:** It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University. You are required to carefully read and sign the form titled "STATEMENT ON ETHICS, PROFESSIONALISM, AND CONDUCT FOR ENGINEERING STUDENTS." If you need soft copy of this statement, email the instructor/GTAs.

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"Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts." (Regents' Rules and Regulations, Series 50101, Section 2.2)

For the first occurrence of academic dishonesty by a student, a zero grade will be given on the exam, report, assignment, or project, as the case may be. Second occurrence of academic dishonesty by the same student (individual or in a team) will result in automatic reduction of one grade letter in the final grade of the course. The Office of Student Judicial Affairs will be informed in writing of academic dishonesty cases.

Plagiarism has many shapes, but can be explained in a few examples under the scope of this course. It maybe presenting someone else's published words (and work) in a way that these words (and works) do not clearly show the source. Any text from someone else's work can not be used "verbatim" unless in double quotes and followed by a citation and appropriate credit. If in doubt, ask the instructor/GTAs.

**Student Support Services Available:** The University of Texas at Arlington supports a variety of student success programs to help you connect with the University and achieve academic success. These programs include learning assistance, developmental education, advising and mentoring, admission and transition, and federally funded programs. Students requiring assistance academically, personally, or socially should contact the Office of Student Success Programs at 817-272-6107 for more information and appropriate referrals.

**E-Culture Policy:** The University of Texas at Arlington has adopted the University email address as an official means of communication with students. Through the use of email, UT-Arlington is able to provide students with relevant and timely information, designed to facilitate student success. In particular, important information concerning registration, financial aid, payment of bills, and graduation may be sent to students through email.

All students are assigned an email account and information about activating and using it is available at [www.uta.edu/email](http://www.uta.edu/email). New students (e.g. first semester at UT-Arlington) are able to activate their email account 24 hours after registering for courses. There is no additional charge to students for using this account, and it remains active as long as a student is enrolled at UT-Arlington. Students are responsible for checking their email regularly.

The instructor/GTAs will send important course-related information to your UT-Arlington e-mail address ONLY. Your email to the instructor/GTA should also come from a UT-Arlington email account. Your email message sent from non-UT-Arlington accounts may never reach the instructor/GTA. You will be responsible for any misplaced or misdirected email that is sent from non-UT-Arlington email address.

**Grade Grievance Policy:** If you have any grievance regarding a grade, consult with the instructor/GTAs. Information about the UT-Arlington grievance policy is at [http://www.uta.edu/gradcatalog/general\\_info#grievances](http://www.uta.edu/gradcatalog/general_info#grievances)

**Final Review Week:** A period of five class days prior to the first day of final examinations will be designated as FINAL REVIEW WEEK. The purpose of this week is to allow UT-Arlington students sufficient time to prepare for final exams. During this week, there will be no schedule or required activities such as field trips, seminars, or performances; and no themes, research problems or exercises of similar scope that have a completion date during or following this week will be assigned unless specified in the class syllabus. During Final Review Week, no exams constituting 10% or more of the final grade will be given, except make-up tests and

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laboratory examinations. In addition, no portion of the final exam will be given during Final Review Week.