University of Texas Arlington
Department of Electrical Engineering

Nanotechnology – Microelectromechanical Systems
Ph.D. Diagnostic Examination

FALL 2008 – November 15, 2008

	To be filled by the student	***To be filled by the graders***		
Question #	**Check to have this question graded. Check only 2.**	**Grade**	**Grade**	**Average**
1				
2				
3				
			TOTAL:	
			GRADE OUT of 100:	

1. The gate oxide for a CMOS process on <100> silicon is to have a thickness of 30 nm.
    a. Calculate the time required to grow this oxide at 900^0C using wet oxidation.
    b. Repeat for 1000^0C using wet oxidation.
    c. Does either of these possible processes seem to be controllable? If so, which one.
    d. In order to achieve high quality ultra-thin gate oxide, discuss the trade-offs of the following process variables: (i) wet or dry oxidation? (ii) Low temperature or high temperature oxidation? (iii) low pressure or high pressure oxidation?

Note: For parts (a) and (b) use the plot below.

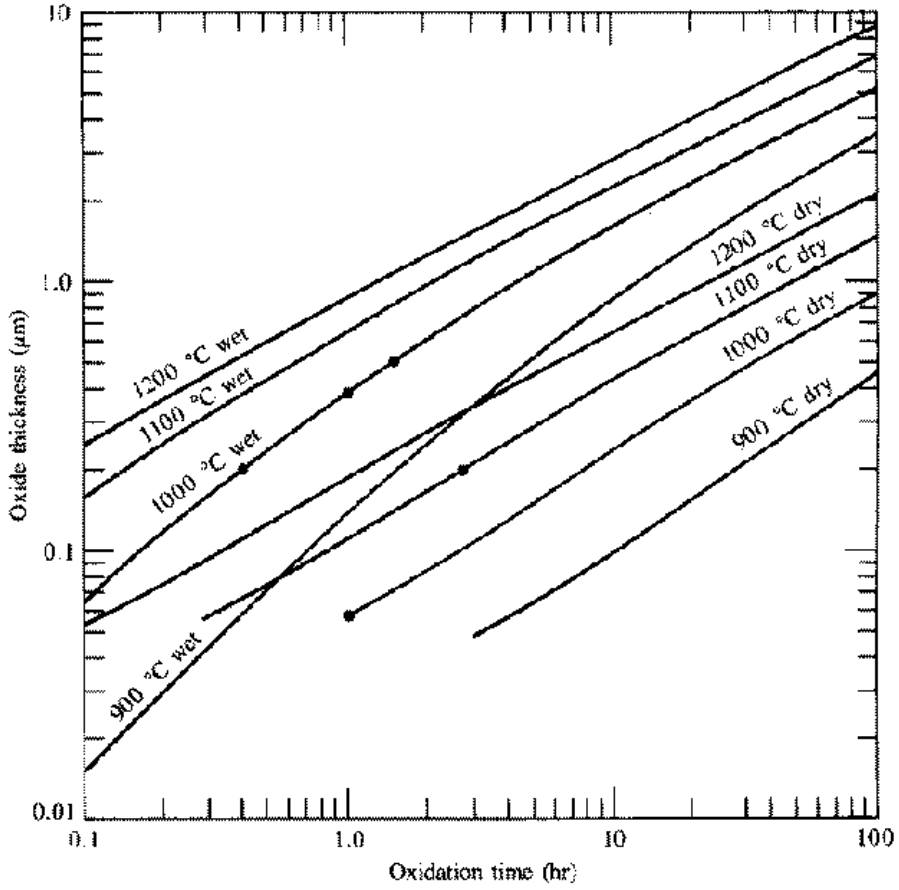
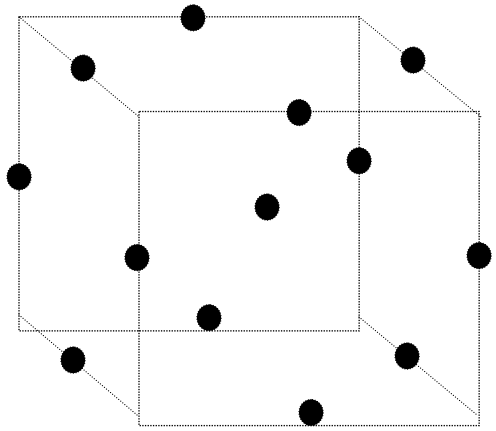


Fig. 3.6 Wet and dry silicon dioxide growth for ⟨100⟩ silicon calculated using the data from Table 3.1.

2. The cubic unit cell of the crystal shown below is composed of 12 atoms positioned halfway along each edge of the cell and one atom at the center of the cell as shown below.

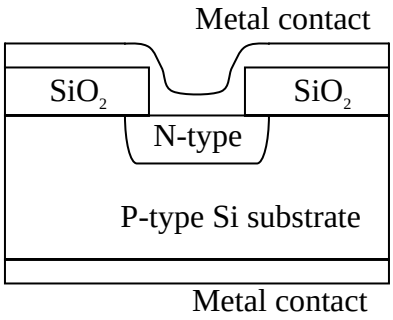


a. How many atoms are there per unit cell?
b. If the lattice constant a = 5.6 Å and the atomic weight is 28 g/mole, determine the density of the material. (Avagadro's no. = 6.03×10^{23} $mole^{-1}$)
c. What is the more common name of this unit cell?

3. Formulate a detailed process flow of the fabrication steps needed to manufacture a p-n junction. Start with a p-type Si(100) wafer. (20 points)

   Final Structure:

Use the next page to draw the fabrication process flow. Explain each step with a single sentence under the Figure.



(a)

(e)

(b)

(f)

(c)

(g)

(d)

Continue on next page if you need more space…