High Current Analog Bipolar Junction Transistor
Amplifier Integrated Circuit Development

Statement of Work for the UTA project with
National Semiconductor Corporation
January 2002 to December 2003

I. Thermal Modeling of Devices
   A. Determination of intrinsic device self-heating and thermal model algebra and topology
      1. Static Model
         a. Analytical models for thermal resistance of discrete square and stripe devices
         b. Experimental determination of thermal resistance of discrete square and stripe devices
         c. Static self-heating model development for discrete square and stripe devices
         d. Transition of thermal resistance model as device changes modes of operation, i.e. forward to saturation, etc.
      2. Dynamic model development
         a. Analytical models for thermal capacitance of discrete square and stripe devices
         b. Experimental determination of thermal capacitance of discrete square and stripe devices
         c. Time dependent self-heating model development for discrete square and stripe devices
         d. Consideration of the time-dependent self-heating interactions with circuit model for the device, beginning particularly with the parameters which affect the base-emitter voltage and beta
   B. Verification and development of ic device model algebra and topology
      1. Circuit related self-heating model
         a. Thermal resistance and capacitance for ic device layouts (wrapped and meshed devices)
         b. Inter-device heating and thermal feedback (through interconnects and/or wafer)
      2. Interconnect thermal model determination and verification
      3. Consideration of variation of device thermal resistance model parameters with different layout (stripe, wrapped, or meshed devices)
   C. SPICE simulation developments - user defined models for thermal effects
      1. Development of thermal feedback driven device temperature calculation sub-circuit
      2. Development of user defined circuit elements to calculate individual device self-heating and interconnect thermal feedback heating
         a. Self heating simulation accomplished by use of a subcircuit operating at a temperature determined by a temperature simulation circuit element
         b. Inter-device heating simulation accomplished by use of multiple subcircuits operating at temperatures determined by temperature simulation circuit elements

II. Amplifier Design and Development (considering push-pull, class AB, common emitter and emitter follower designs)
   A. Comparison of circuit topologies considering
      1. Optimization of output swing
      2. Reduction of zero-crossing non-linearities by evaluating effects of different schematic topologies
      3. Soft saturation schemes such as use of clamps to minimize degree of saturation
   B. Comparison of layout topologies, considering variation of ic topologies for
      1. Interconnect delay optimization
      2. Circuit bandwidth optimization
      3. Optimum thermal response using isothermal layout
      4. Controlling heat flow by design of metallization
   C. Bias schemes
      1. Comparison of the effectiveness of selected bias schemes for amplifier design, considering
         a. Current mirror
         b. Vbe multiplier
         c. Diode bias
         d. Resistor ballast
      2. Application of thermal model simulation and variation of thermal feedback to determine optimum bias schemes for reduction of thermal runaway, considering

a. Negative thermal feedback schemes which maintain constant current by matching thermal characteristics
b. Thermal compensation schemes like the band-gap reference
c. Limitation of thermal runaway by ballast resistors

III. Deliverables
  A. Models as defined in I
    1. Thermal model equations and operating domain
    2. Thermal model parameter extraction and optimization schemes
    3. As applied to
      a. Intrinsic device model
      b. Integrated circuit devices
  B. Amplifier circuits considered including push-pull, class AB, common emitter and emitter follower designs
  C. Circuits - procedures for and determination of practical optimum for
    1. Output swing
    2. Zero-crossing non-linearities
    3. Soft saturation
  D. Layout topologies - design rules for
    1. Minimum delay
    2. Maximum bandwidth
    3. Heat management
  E. Bias schemes (as in II.C.1 and II.C.2) - design rule models for
    1. Bias schemes
      a. Current mirror
      b. Vbe multiplier
      c. Diode bias
      d. Resistor ballast
    2. Mitigation of thermal runaway by temperature matching and compensation.

IV. TDT Project Objectives
  A. Yield prediction tool using circuit layout and process characterization data
  B. MTTF prediction using local temperature determined metal migration computation
  C. Figure of merit for aggregate comparison of circuit performance relative to the behavioral description of the component