Surface Micromachining of Uncooled Infrared Imaging Array Using Anisotropic Conductive Film

Weiguo Liu, Lingling Sun, Weiguang Zhu, Ooi Kiang Tan

Microelectronics Center, School of Electrical and Electronic Engineering
Nanyang Technological University, Singapore 639798

ABSTRACT

Micromachining processes have been extensively adapted in developing uncooled infrared imaging array. One of the most important sensing materials in the array is ferroelectric thin film. To integrate the ferroelectric thin film with the signal processing circuitry, an IC compatible process has to be applied. Various methods have been successfully used to prepare high quality oxide ferroelectric thin films. Unfortunately, not all of the methods are compatible with a standard CMOS process. None of them can optimize the ferroelectric thin film after it has been deposited onto IC chip due to high heat treatment temperature. A Flip-Chip Transfer (FCT) method is proposed here to optimize the ferroelectric thin film separately with the IC chip. Doing so, any necessary measure could be taken to optimize the performance of the ferroelectric thin film. After that, anisotropic conductive film (ACF) is applied between the ferroelectric thin film and the IC chip to establish interconnection and mechanical bonding between the sensing element and the signal processing circuit. Micromachining process is then applied to remove the substrate, usually Si, on which the sensing material is deposited. A 128x1 linear pyroelectric infrared imaging array is being fabricated.

Keywords: Surface micromachining; Flip-chip transfer; anisotropic conductive film; Pyroelectric infrared imaging array

1. INTRODUCTION

Thermal detectors include bolometers and pyroelectric detectors. These detectors typically operated at room temperature (uncooled) and do not require cryogenic cooling. Thermal detectors today show many good characteristics, such as fast response, low noise, low power consumption, and moderate sensitivity at ambient temperature. The detector signal is related to the temperature of the detector material, which is altered because of incident thermal radiation. Both pyroelectric and bolometer arrays are being developed and at present there is no clear preferred technology. To improve the sensitivity, thermal structure of the detector plays an important role. Different configurations of the uncooled infrared imaging arrays have been proposed based on different silicon micromachining techniques. Micro-bridge and micro-air-gap structures have been realized using Si surface micromachining. Micro-bridge structure has been proved to be successful for the resistive bolometers, in which, the deposition of resistor array could be carried-out at a temperature compatible with a standard CMOS process. To improve the levels of performance of the bolometer arrays, materials with higher temperature coefficient of resistance (TCR) are required. Recently, high temperature superconductors and colossal magneto-resistive materials are examined. These materials may be deposited at a temperature not compatible with the standard CMOS process. Among pyroelectric materials, ferroelectric thin films are the most promising. When ferroelectric thin films are used as thermal sensing materials, one important factor has to be considered in the fabrication of the arrays is the compatibility of the micro-fabrication process of the device with the CMOS processes.
In this paper, we propose a new process to provide the opportunity to optimize the thermal sensing materials for either bolometer or pyroelectric arrays separately with the CMOS process. As an example, pyroelectric array with ferroelectric thin film as sensing material is being developed using the proposed flip-chip transfer (FCT) surface micromachining technique. This method is applicable to the fabrication of both the bolometer and the pyroelectric uncooled infrared imaging arrays.

2. FERROELECTRIC THIN FILM PREPARATION

Ferroelectric thin films have been proven promising materials in developing pyroelectric uncooled infrared imaging arrays. Many techniques have been researched for ferroelectric thin film deposition. These include chemical solution deposition, such as sol-gel or metal-organic deposition, sputtering, pulsed laser ablation deposition and metal-organic chemical vapor deposition (MOCVD). Each of the methods has its own advantages and disadvantages. High deposition or post-deposition annealing temperature makes these methods not compatible with a standard CMOS process. Efforts have been paid either to reduce the deposition temperature or find a novel integration process to avoid the impact of the high temperature on the CMOS process. Recent progress in MOCVD deposition of ferroelectric lead zirconate titanate (PZT) thin films at low-temperature is quite encouraging. But unfortunately, not all ferroelectric thin films could be deposited at a temperature lower than 450°C, which is the upper limit on the ferroelectric thin film process temperature required by the CMOS process. Ferroelectric thin films deposited at relatively low temperatures show poor crystallinity and thus poor pyroelectric property. To optimize the properties of the ferroelectric thin films, high deposition temperature or high post-deposition annealing temperature is desirable. In this paper we show that dielectric and pyroelectric properties of lead zirconate titanate (PZT) and lead titanate (PT) multilayered thin films can be optimized at a temperature around 600°C.

Substrate used in this work is <100> n-silicon wafer that is first thermally oxidized to form 500nm SiO2 on both sides of it. 200nm Si3N4 is then deposited onto both sides of the wafer by LPCVD method. On the front side, 50nm Ti is deposited followed by 150nm Pt to serve as bottom electrode for the PZT and PT thin films. Spin-coating process of PZT and PT thin film is performed on the top of the Pt thin films. Moisture-insensitive solid PZT and PT precursors are prepared from partially stabilized titanium isopropoxide, lead acetate trihydrate and zirconium acetylacetone without any solvent. The solid precursors are dissolved in 2-methoxyethanol to form sols. The sols are used to prepare PZT and PT thin films. Chemicals used in the experiments are acetylacetone (Fluka Scientific), lead acetate trihydrate (Riedel-de Haën), zirconium acetylacetonate (Fluka Scientific), and titanium isopropoxide (Sigma-Aldrich). After the precursor is formed, 2-methoxyethanol is used as solvent to prepare PZT and PT sols with different concentrations. The thin films are prepared with spin-coating process at 3000rpm for 30 seconds. The spin-coating process is repeated till desired thickness is reached. Each layer is pre-baked at certain temperature for 2 minutes by putting the film directly into pre-heated Thermolyne 47900 furnace after the film is spin-coated. Annealing of the films is carried out at 600°C for 30 minutes. Details of the thin film preparation process was reported elsewhere. Multilayered PZT/PT thin films are prepared by alternatively depositing PZT and PT layer for 5 times, and finally a PZT layer is deposited with the PZT as the first and the final layer in the multilayered thin film. In addition, PZT thin films alone are also prepared by repeating the spin-coating steps for 11 times. The fired thickness of each layer of PZT or PT thin film in one spin-coating step is about 50 nm, thus, total thickness for both the PZT/PT and the PZT thin film is about the same of 550 nm.
We find that prefer orientation of PZT thin films is strongly influenced by the pre-baking temperature of the films when they are deposited. Results are shown in figure 1. If the pre-baking temperature is lower than 500°C, randomly oriented films are obtained (figure 1(a)). When the film is pre-baked at 500°C, (001) prefer oriented film is obtained as shown in figure 1(b).

![XRD patterns of PZT thin films pre-baked at different temperatures.](image)

The dielectric measurement results are given in Figure 2. It is seen that the multilayered PZT/PT thin film exhibits a relatively lower dielectric constant than that of the PZT thin film due to the low dielectric constant of the PT film. This result can be well described by considering the PZT and PT thin films as two capacitors in serial.

![Dielectric constant and loss of (a) PZT and (b) PZT/PT thin films.](image)

![Voltage responses of PZT and PZT/PT thin film detectors (a) waveforms and (b) responsivities.](image)
Due to its relatively low dielectric constant, PZT/PT multilayered thin film shows high dynamic pyroelectric responses compared with those of the PZT thin film prepared under identical conditions. Figure 3 shows the differences between the responses from PZT/PT and PZT thin films.

The pyroelectric coefficients of PZT/PT and PZT thin films near room temperature are about 380 and 400 $\mu$C/m$^2$K respectively. The figures of merit of PZT/PT and PZT thin films are calculated using the measured dielectric properties and pyroelectric coefficients of those films. Parameters used in the calculation and the calculated results are listed in Table 1. Where, $F_v$ and $F_D$ are voltage response figure of merit and detectivity figure of merit respectively.

### Table 1  Figures of merit and the parameters used in calculation.

<table>
<thead>
<tr>
<th></th>
<th>Pyroelectric coefficient $p'$ ($\mu$C/m$^2$K)</th>
<th>Relative dielectric constant $\varepsilon_r$</th>
<th>Dielectric loss $\tan\delta$</th>
<th>Volume heat capacity $c'$ ($10^6$ J/m$^3$K)</th>
<th>$F_v = \frac{p'}{c'} \varepsilon$ (m$^2$/C)</th>
<th>$F_D = \frac{p'}{c' (\varepsilon \tan\delta)^{1/2}} (10^{-6}$ Pa$^{-1/2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PZT</td>
<td>400</td>
<td>558</td>
<td>0.011</td>
<td>2.9</td>
<td>0.028</td>
<td>18.7</td>
</tr>
<tr>
<td>PZT/PT</td>
<td>380</td>
<td>389</td>
<td>0.012</td>
<td>2.9</td>
<td>0.038</td>
<td>20.3</td>
</tr>
</tbody>
</table>

From all these results, it can be seen that if multilayered PZT/PT thin films are prepared under appropriate conditions, say, 500°C pre-baking and 600°C annealing, these films are good candidate materials for developing high performance pyroelectric IR detectors. Optimizing of the multilayered PZT/PT thin films is still in progress.

### 3. STRUCTURE OF THE 128x1 ARRAY

Figure 4 shows the structure of the 128x1 pyroelectric detector array fabricated with a flip-chip transfer (TCF) process. Two-level micro-structure is utilized. In the top level, PZT/PT thin film is deposited onto silicon nitrite/silicon dioxide membrane first, then the membrane is transferred to the bottom level, i.e., the CMOS fabricated silicon substrate. Interconnection between the pyroelectric thin film and the CMOS circuit is built up through the anisotropic conductive film (ACF). The membrane is finally patterned as a micro-bridge structure as shown in figure 4(A). Pitch size of the array is 100x100 $\mu$m$^2$, pixel size is 80x100 $\mu$m$^2$. Bonding pads are not less than 60x80 $\mu$m$^2$. Since the ACF is quite thick, resonant structure is not applicable in this structure to increase the radiation absorbance. So in this structure, an absorber is applied to increase the average infrared absorption in 8-14 $\mu$m wavelength ranges.
4. FABRICATION OF THE ARRAY

Fabrication of the array takes three major steps: the deposition of the PZT/PT thin film, fabrication of CMOS circuitry, and flip-chip transfer. These steps are summarized in figure 5 to figure 7.

Figure 5 shows the procedure for the deposition of PZT/PT thin film. (A) The bottom electrode Pt/Ti is patterned first. Etchant of the Pt/Ti layer is aqua-regia. Etching mask is AZ1518 photoresist. The etching is carried-out at 80°C. Then the SiN/SiO$_2$ layers are patterned in CF$_4$/O$_2$ plasma. (B) PZT/PT thin film is spin-coated onto the patterned Pt/Ti bottom electrode, and then is patterned using 50:50:1 H$_2$O:HCl:HF etchant. (C) Au top electrode is deposited using a lift-off process.

Figure 6(A) is the as-fabricated CMOS chip. Standard 100x100 µm$^2$ bonding pads are formed and pad windows are left in the passivation layer (not shown in the figure). The next step in the CMOS substrate preparation is the applying of the anisotropic conductive film (ACF). ACF used in this work is 3M Z-axis adhesive film 5552R.\textsuperscript{5} The 5552R film is a dedicated ACF for very fine pitch bonding. The ACF is applied to CMOS substrate under stereomicroscope.

After the pyroelectric thin film and the CMOS circuitry are prepared separately, a FCT process is applied to bond them together. Figure 7 shows the FCT process. Bonding of the 5552R film requires a three part procedures: heat tacking the film to CMOS substrate at temperature 80 to 100°C under 0.1 to 1.5 Mpa pressure for 3 to 5 seconds, removal of the release liner, and bonding the CMOS substrate to the silicon substrate which carries the pyroelectric thin film at 170 to 190°C under 2 to 4 Mpa pressure for 15 to 30 seconds. The alignment is done using a double-side mask aligner. To remove the silicon substrate under the PZT/PT thin film and release the SiN/SiO$_2$ membrane, a single side etching process is applied. The etching-station is shown in figure 8, where the edge of the silicon wafer is sealed to a glass tube with silicone paste, TMAH is used as etchant, concentration of the TMAH is maintained by using a condenser. Etching-back is carried-out at 80°C.
In step (B) of figure 7, the patterned SiN/SiO$_2$ membrane together with PZT/PT thin film is transferred to CMOS substrate after the etching-back of the silicon substrate. Then in step (C), a absorber is designed and deposited to the pixels. The absorber is designed together with the PZT thin film, top electrode, bottom electrode, and SiN/SiO$_2$ membrane. A polyimide layer is spin-coated onto the SiN/SiO$_2$ membrane, and a thin Ni layer is finally deposited to increase the absorptance. Thickness of each layer in the structure is: polyimide-1500nm, Ni-20nm. The Ni layer is patterned during the lift-off process, and is substantially used as the mask to pattern the polyimide layer with O$_2$ plasma.

5. CONCLUSIONS

Flip-chip transfer process provides the opportunity to optimize the ferroelectric thin film separately with the fabrication of CMOS circuitry and allows the integration of the ferroelectric thin film with the CMOS substrate at a low temperature. Results shown in this work prove that the PZT/PT multilayered ferroelectric thin films deposited with sol-gel method show promising pyroelectric properties when the films are appropriately thermal processed.

It is noteworthy that the pyroelectric sensing elements in this present 128x1 array is “face-down” to the CMOS substrate. To examine the infrared absorption property of this structure, IR absorbance in wide wavelength range is calculated. The result is shown in figure 9. It can be seen that the average IR absorbance of the absorber is higher than 70% in 8-14μm ranges and peak absorbance is about 96%, which is better than a single layer metal absorber.\(^6\)

This flip-chip transfer method can also be applied to a “face-up” process. In this process, a third substrate called sacrificial substrate is being used. The membrane together with the PZT/PT thin film is first transferred to the sacrificial substrate, and then the membrane is transferred to the CMOS substrate. This time, the pyroelectric sensing pixels are “face-up”.

6. REFERENCES