Si based multi-layered print circuit board for MEMS packaging fabricated by Si deep etching, bonding and vacuum metal casting

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ABSTRACT

In our previous works, metal injection technique into small diameter (10 -100 \( \mu \text{m} \)) through holes was developed and applied for fabrication of Si based print circuit board. In the present work, we present the metal filling technology by vacuum casting into 3 dimensional through holes and trenches structure fabricated in stacked layered Si wafers prepared by fusion bonding of ICP etched Si wafers. Metal electrical feed through was successfully prepared by the method.

Conventional print circuit boards have been fabricated with Epoxy resin based materials. In recent years Si is regarded as a candidate for next generation materials for print circuit board substrates, as the substrate whose thermal elongation same as the mounted chips is an ideal solution to residual stress problems in the elevated temperature application. In this report, we developed the double sided mountable stacked circuit board using Si deep etching technology and fusion bonding. This technology is expected to lead to the realization of the assembling of sensors, actuators and ICs, i.e. 3 dimensional MEMS packaging.

In this report, we adopted micromachining technology to this application area and the special emphasis is placed on the low cost and reliable process development. The detailed items to be developed are shown as follows;

1. Development of Si wafer through holes penetration and trench formation by ICP etching.
2. Alignment and bonding of micromachined wafers
3. Development of insulating layer with oxidation
4. Development of formation of electrical feed through for stacked layers

Keywords: Deep Reactive Etching, Through Hole, Fusion bonding, Electrical feed through, Vacuum metal casting

1. INTRODUCTION

There is an increasing demand for high density packaging and the trend needs the fine pitch electrical feed through for the mounted devices. This technology is expected to lead to the realization of the assembling of sensors, actuators and ICs, i.e. 3 dimensional MEMS packaging. A schematic image of the stacked structure of Silicon boards to be developed is illustrated in Fig. 1

The through holes have been fabricated with Laser, Ultrasonic, and Electro-discharge machining techniques. The diameters of the through holes made by these methods are generally larger than 50 \( \mu \text{m} \) and the aspect ratios are less than 5. However in recent years, with the advancement of the micromachining technology such as ICP etching and SR deep lithography, small and high aspect ratio through hole and trench etching has been realized. Extensive studies have
been already accomplished in Si deep etching, insulation technology, and localized metallization technology. Recently these technologies are applied to 3-D integration and packaging (3) and data storage MEMS devices fabrication (4, 5). In this report, we adopted micromachining technology to this application area and the special emphasis is placed on the low cost and reliable process development. The detailed items to be developed are shown as follows:

1. Development of Si wafer through holes penetration with the diameter of 40µm and trench formation by ICP etching.
2. Alignment and bonding of Micromachined wafers
3. Development of insulating layer with oxidation
4. Development of economical method of formation of electrical contact feed through for stacked layers with metallization by electro plating, vacuum casting and metal powder injection molding

Finally the fabricated substrate was evaluated by insulation testing.

2. EXPERIMENTAL

2.1 Penetration and trench etching of Si wafer and cost effective mask production

Silicon substrate was penetrated and trench etched by deep reactive ion etching using STS ICP machine. The optimum etching conditions were investigated to have smooth and vertical penetration holes with as smallest diameter as possible. Several mask preparation methods are evaluated from the viewpoint of cost reduction. The thickness of the Si wafer was 400µm. Conventional mask was prepared by resist structure (2µm) and thermal oxide (2µm). Thick resist is necessary for penetration of Si wafer. For thicker mask, (1) two times spin-coated resist, (2) etching from both sides and (3) SU8 resist methods are employed and evaluated.

2.2 Alignment and bonding of micromachined wafers

The processed wafers can then be aligned using an Electronic Vision Group EV640 wafer aligner after chemical cleaning with H₂SO₄ + H₂O₂ solution, designed to achieve one-micron alignment accuracy. The 4 micro machined wafers are then bonded in the furnace at the temperature of 1100 degree C by conventional fusion bonding technology. The bonding of the processed wafers with ICP was usually difficult because of the deposition of the passivation layers onto the backside of the wafer during Bosch process. The difficulties of the contamination could be avoided by protecting the backside of the wafer by resist during ICP etching process.

2.3 Formation of insulating layers

Insulating layers were prepared by thermal oxidation (wet oxidation 1100 degree C x 20 hr) to form 2 µm thick oxide. Insulating resistance was measured for evaluation of the insulating layers using pA meter (Hewlet Packard 4140B). The measured temperature and humidity was 26 degree C and 56% respectively. The probe employed was made of W. The Si wafer (4 inch) was type n, thickness 400 µm and the sheet resistance of 8 to 12 (Ωcm).

2.4 Formation of electrical contact with metallization by electro plating, vacuum casting and metal injection molding
Electrical feed through was formed using the following methods;

(1) Electro plating method
Si wafer was deposited with Cr/Au to serve as a base substrate for electroplating. Photo resist was spin coated and the substrate with though holes are attached. UV light was exposed and developed to expose the base Au/Cr electrode layer. After rinse and drying, the through holes are filled with Ni to make electrical contacts.

(2) Vacuum casting method
Low melting point metal was employed to make electrical contacts. First the surface of the Si wafer with through holes was covered with polyimide tape. Low melting point (90 degree C) metal with the same material spacer was placed under the Si wafer. The whole system on a hot plate was heated after evacuation. After melting the metal, completely atmospheric pressure was introduced to let the melted metal enter into the feed through. After cooling, the unnecessary part was removed from the surface. Polishing and wipe out methods were employed for removal of the metal.

(3) Powder injection method
The electrical feed through was fabricated by casting the Ag (80 wt%) + Cu (20 wt %) mixed with binder into the small diameter through holes in oxidized Silicon wafer. A multi-component binder system comprising of EVA (Ethylene Vinyl Acetate 35 wt%) + PW (Paraffin Wax 65 wt%) and PAN were used. Super critical debinding method is applied prior to final sintering process. The ratio of metal powder and binder was 9:1. The metal insert process employed here was as follows;
   (1) Wafer was cut by dicing saw into 20x20 mm
   (2) Mixture of binder and metal powders at elevated temperature (120 degree C)
   (3) Metals powder binder coating and injected into through hole with pressing
   (4) Removal of unnecessary part (wipe-out method)
   (5) De-binding (Conventional and Super critical methods) and final sintering in the furnace at 700 degree C
Conventional de-binding process includes heat treatment as follows;
Room temperature to 250 °C, 9 hours, 250°C x 2 hours, 250 to 450°C 8 hours, 450 °C x 4 hours, 450 to 750°C 8 hours, 750°C x 2 hours.

(4) Pseudo isostatic pressing method.
This method is similar to the vacuum casting method. The sample with through holes was introduced in a vacuum chamber with metal power of Tin in a closed tube. After evacuation, the sample was heated to melt the Tin and pressure was applied to induce isostatic pressure not to break the brittle Si structure. The Tin metal was introduced into the thorough holes with the pressure.

3. RESULTS AND DISCUSSIONS

3.1 Cost effective Mask preparation Technology for Deep RIE

Fig.2  Cross Sectional View of Si Substrate

Fig.3 Cross Sectional View of the Substrate Etched by 2 Times Coated Photo Resist (Thickness 400 µm)
Selectivity of photo resist mask to Si was measured as 60 and that of SiO₂ to Si was about 120. The mask consist of 2 µm photo resist and SiO₂ (1.8µm) could be used for Si deep etching of 340 µm and penetration was not possible by this mask as shown in Fig. 2. Two times of spin coating was applied to make thicker layer of the photo resist. As shown in Fig. 3, the cross sectional view of the etched substrate by the double layer exhibits the stepped structure. This is resulting from the stepped structure of the photo resist. This is because the first coated layer baked two times which resulted in difference of developing in two layers. Photo resist coating and etching from both sides was also tried but the cross section obtained has also resulted in the stepped structure. Fig. 4 shows the SEM image of the processed through holes and trenches structure fabricated by ICP etching from both sides, and Fig. 5 shows the plane view of the processed wafer.

Thick resist of SU-8 was also evaluated as a masking material. In this case no oxide mask was used. By spin coating of 500 rpm/10 sec and 2000rpm/15sec, 25 µm thick mask was obtained. This mask is very convenient and no need to oxidize nor HF etching. The only problem is the removal of the mask after the etching. Acetone was not effective to remove. The mixture of H₂O₂ and H₂SO₄ at 100 degree C was effective for removal. This method would not be used if we have metal layer.

3.2 Evaluation of etching conditions

Various etching conditions were investigated in Deep RIE to do etching of small diameter and high aspect ratio through holes. Typical etching rate was 3 µm/min. Diameter of less than 30 µm was very difficult to do penetration. Etching depth of through holes more than 50 µm diameter is linearly dependent on time.

3.3 Bonding of micromachined wafers
Fig. 6 shows the cross sectional view of processed four wafers aligned and then fusion bonded. Each wafer was etched to make through holes and trenches. The bonding was so successful that the bonded interface could not be identified by the SEM observation. The alignment accuracy was within 5 µm. Described before, the bonding of the processed wafers with ICP was usually difficult because of the deposition of the passivation layers onto the backside of the wafer during Bosch process and the presence of residual humidity caused by wet cleaning. The difficulties of the contamination could be avoided by protecting the backside of the wafer by resist during ICP etching process. The humidity was also eliminated by proper drying process. Fig. 7 shows the plane view of the bonded two wafers taken by infrared imaging. Part of the wafers was not bonded because of the presence of the contamination.

Fig. 7 Plane IR image of the bonded wafers with through holes and trenches structure and imaging apparatus

Fig. 8 Cross sectional SEM images of the metal filled through holes and trenches structure
3.4 Formation of electrical contact with metallization

Shown in the previous study (2), the metal filling with electroplating is time consuming and needs special technique. As observed, some of the through holes are not filled with metal. The reason of the void was resulting from the lack of the electrolyte supply in the small diameter holes. The metal filling in the case of multi layered stack structure was much more difficult compared with the single layer.

Fig. 8 shows the cross sectional views of the structure filled with Tin metal by vacuum casting method. As shown in the picture, the electrical feed through was formed. Some of the pictures show that the part of metal was dropped from the through holes during dicing process for observation. In this method the removal of the metal on the unnecessary part is the problem. If we remove by polishing, the oxide layer is also removed. Selective polishing method should be developed. Another problem is that the material has low melting temperature and we cannot use the device at the elevated temperature.

The through holes are filled with metal powders. Fig. 9 (a,b) shows the cross sectional and plane view of the Si wafer. Conventional debinding process resulted in scattering the metal powder onto the Si wafer during debinding process and final sintering process. Very slow temperature elevation heating and super critical debinding process resulted in good formation of electrical feed through. As indicated in Fig 9 (a), the feed through formed with small bumps because of expansion of the metal powder area. This is assumed to be volume expansion of Cu by oxidation. The electrical conductivity test was sufficient between top and bottom for a single wafer. However electrical conductivity for 4 wafers

<table>
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<tr>
<th>Requested technology</th>
<th>Accuracy</th>
<th>Technological difficulty</th>
<th>Facility investment</th>
<th>Time</th>
<th>Problem</th>
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<tr>
<td>Electroplating</td>
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<td>Difficult</td>
<td>Electroplating bath</td>
<td>Several hours</td>
<td>Removal of electrode Cleaning</td>
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<tr>
<td>Vacuum casting</td>
<td>Good</td>
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<td>Vacuum chamber and pump</td>
<td>Short time</td>
<td>Removal of unnecessary part Not suitable for high temperature use</td>
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<tr>
<td>Powder injection method</td>
<td>Good</td>
<td>Simple</td>
<td>Press Sintering furnace</td>
<td>Long</td>
<td>Shrink Long Debinding time</td>
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Table 1. Comparison of Metal filing methods
bonded structure was much lower than the evaluated value. This is mainly because the metal was not well supplied for stacked structure. Observation shows the shrinkage of the sintered structure resulted in the discontinuity of electrical feed through. Also the electrical isolation between holes was not sufficient in some cases. This is attributed to the metal evaporation and re-adsorption onto surface. The more investigations are to be done for the isolation. Several Feed through formation methods have been proposed. The electroplating and vacuum casting method are well known processes. Compared with these methods, this is rather rapid and economical, and provides desired shape of bumps and no need of eliminating the unnecessary part. Table 1 summarizes the methods proposed. Vacuum casting method is most convenient, but the application area is limited because of the low melting point. The quality of electroplating must be increased, but the time necessary for completing the filling the through holes is too long from the industrial point of view. Powder injection method proved to be cost effective and reliable.

### 3.5 Evaluation of Fabricated Substrate

Fabricated substrates using ICP etching and Powder injection method were tested by the probing system as shown in Fig. 10 and measured data are summarized in the table 2. The resistance calculated with measured value was much higher than 1 GΩ. The values are satisfactory and the fabricated device was proved to be cost effective method. Voltage of 100 V was applied safely without any electrical break down. However as described earlier, electrical conductivity for 4 wafers bonded structure was much lower than the evaluated value. This is mainly because the metal was not well supplied for stacked structure. In this study we tried the metal filling after bonding the all wafers. However the bonding must be performed after filling the metal into each wafer.

To establish the basic technology for the next generation circuit board substrate, the fabrication method for through hole etching and metal filling was developed. The Si wafer, which has the same thermal coefficient as mounted chips, of 4 inch size was used and we have fabricated the electrical feed through by filling the metal into the small holes prepared by ICP etching. Moreover the wafers with through holes and trenches were aligned and bonded to make the stacked layer structure and we had tried the metal filling into the holes and trenches. The fabricated device was tested by insulation measurement. These are summarized as follows;

1. Deep etching of less than 40 µm diameter through holes and trenches are etched in Si wafer with ICP machine

<table>
<thead>
<tr>
<th>Evaluation of Fabricated Substrate</th>
<th>1</th>
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<tr>
<td><strong>Applied Voltage (V)</strong></td>
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<tr>
<td><strong>Resistance (GΩ)</strong></td>
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<td>6.7</td>
<td>10</td>
<td>12.5</td>
<td>20</td>
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Table 2 Evaluation data of the fabricated board
The wafers are aligned within the accuracy of 5 \( \mu m \) and bonded by fusion bonding to make multi layered structure.

The insulating layer of more than 1 G\( \Omega \) was obtained.

Injection molding and vacuum molding were applied for fabrication of electrical feed through. The complete filling of the metal into complicated structure is to be established.

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Reference


