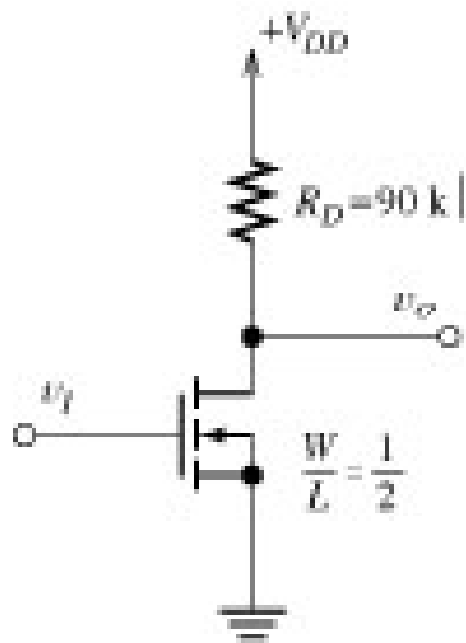
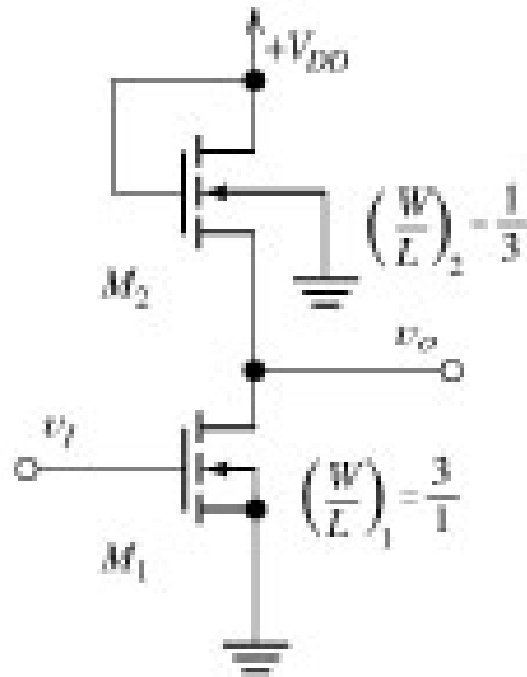


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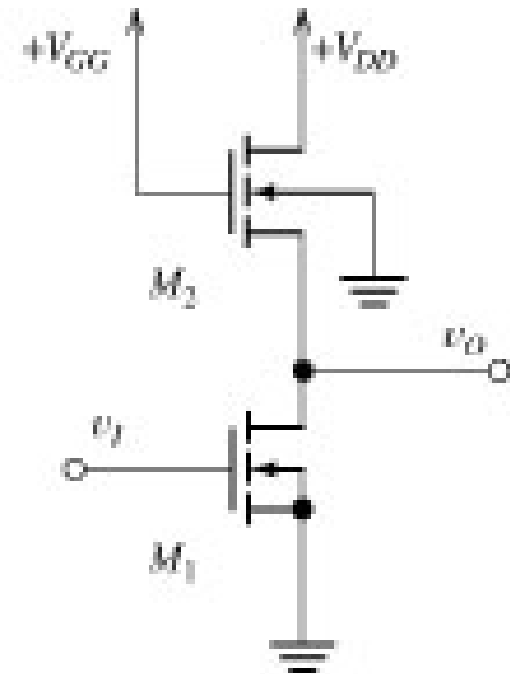
Professor Ronald L. Carter
ronc@uta.edu
<http://www.uta.edu/ronc/>



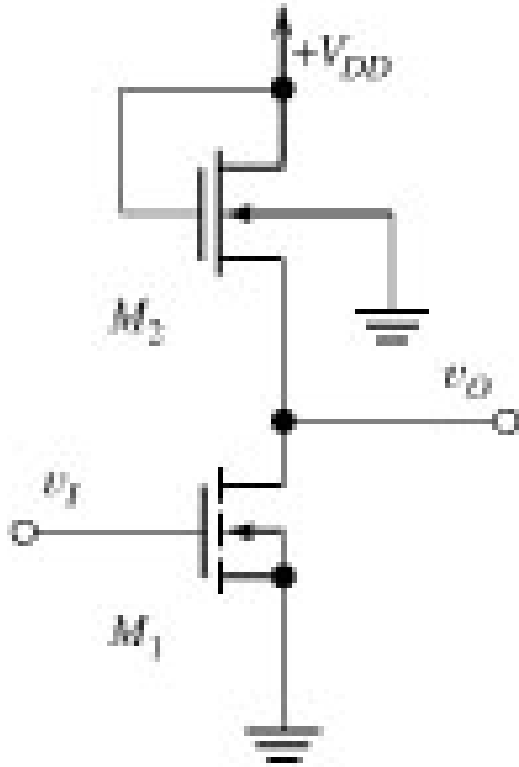
(a) Resistive pull-up



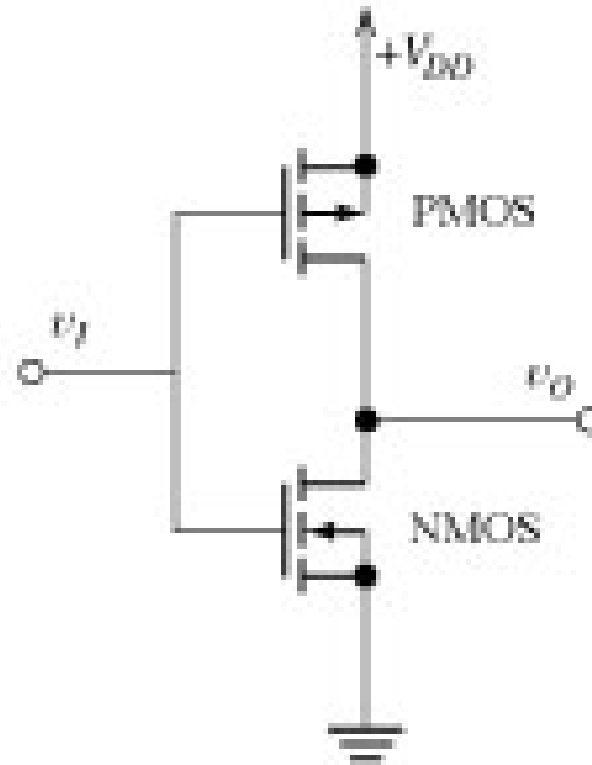
(b) NMOS pull-up



(c) NMOS pull-up with bias source



(d) Depletion-mode NMOS pull-up



(e) CMOS

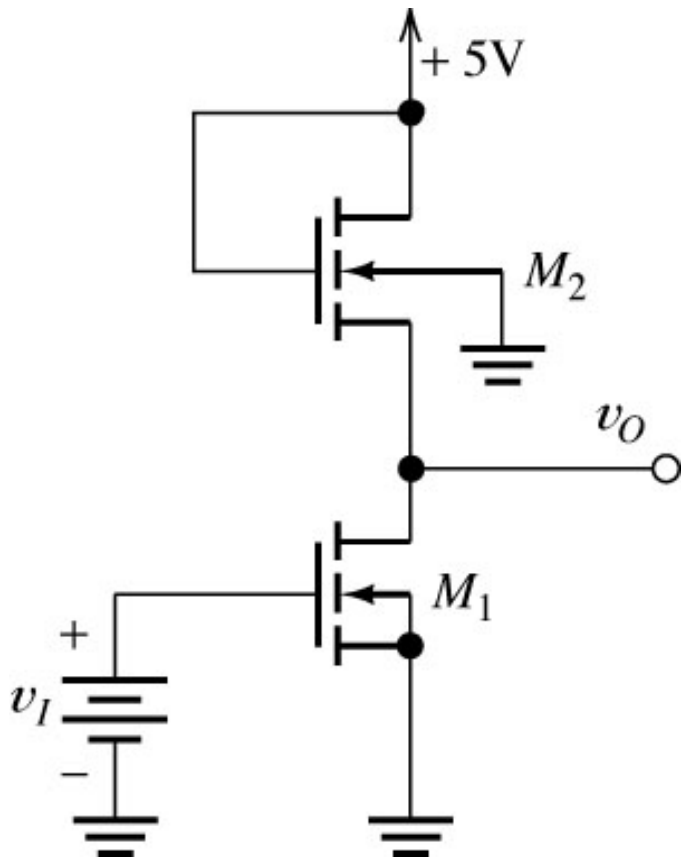


Figure 6.26 Circuit for Example 6.6.

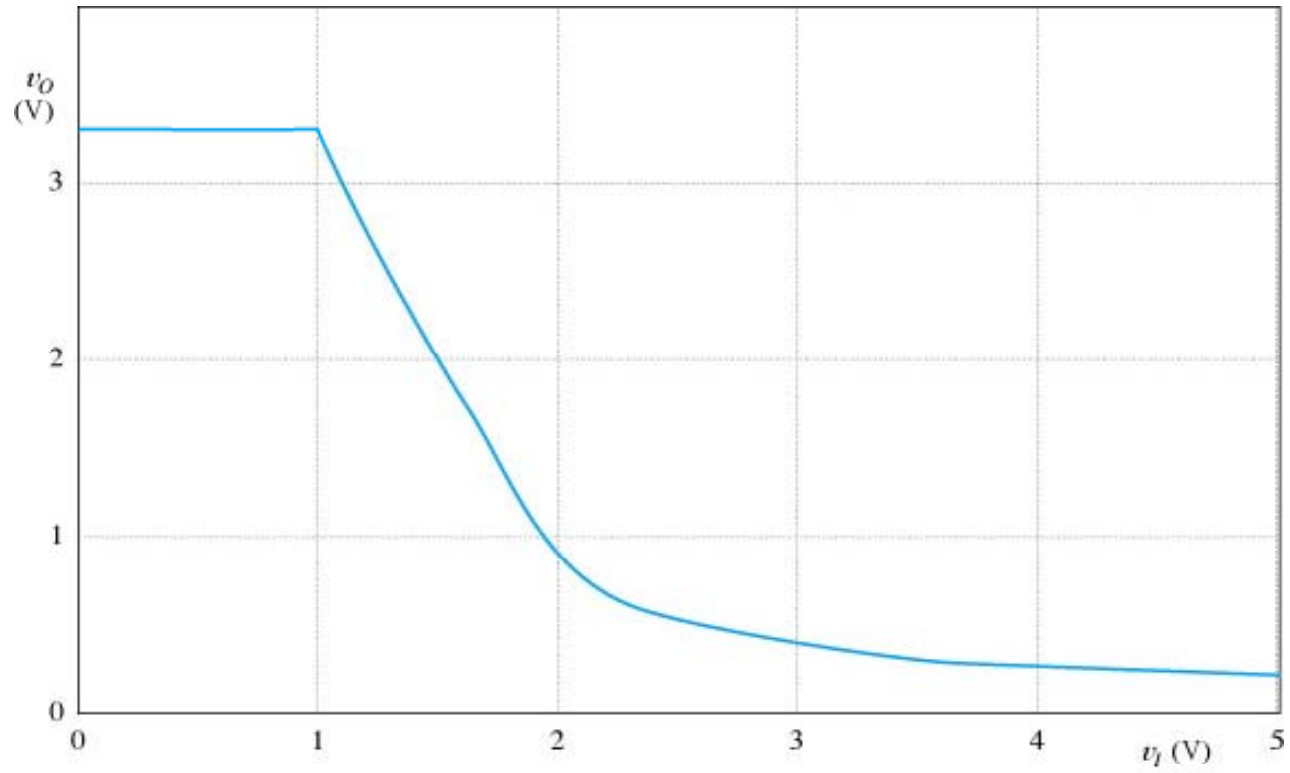


Figure 6.29 Transfer characteristic of the NMOS pull-up inverter.

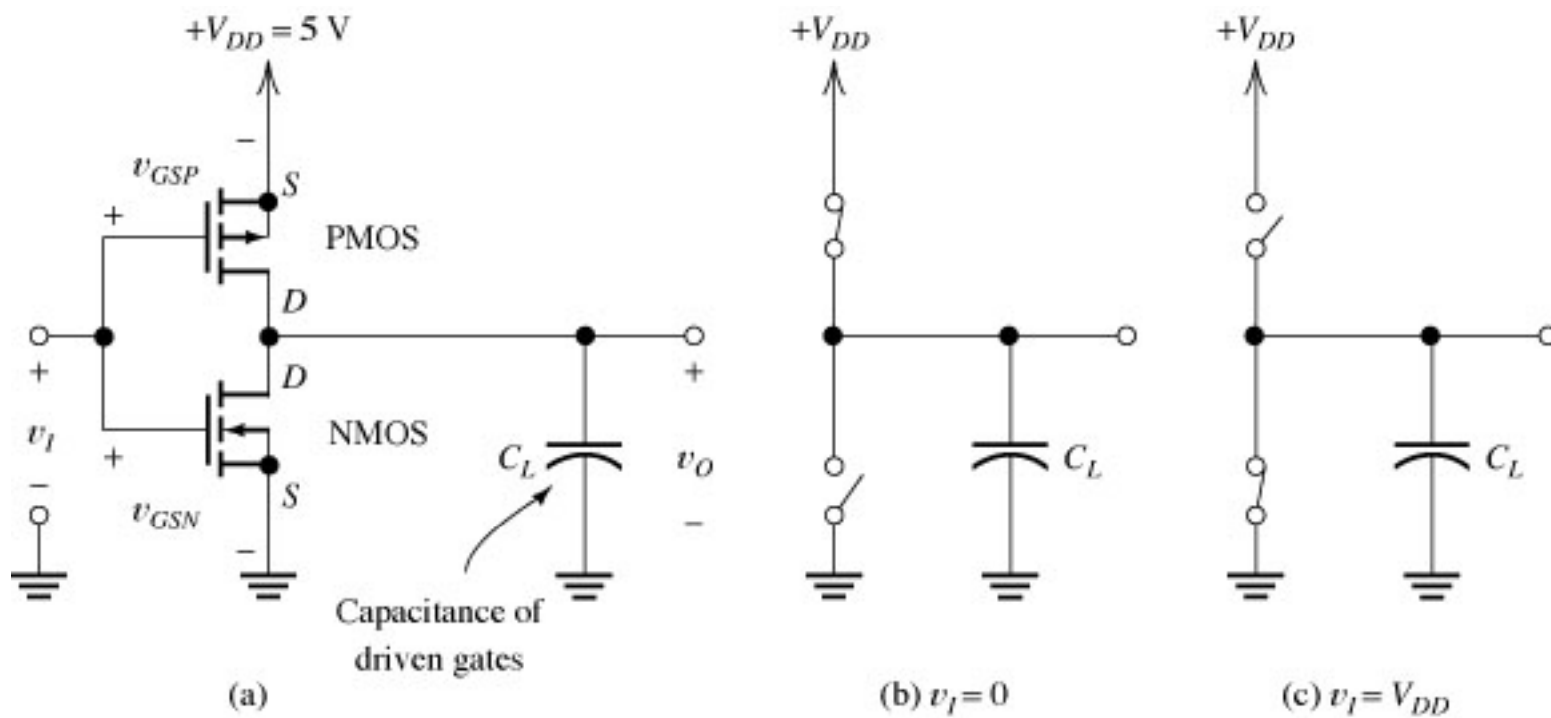


Figure 6.30 CMOS inverter.

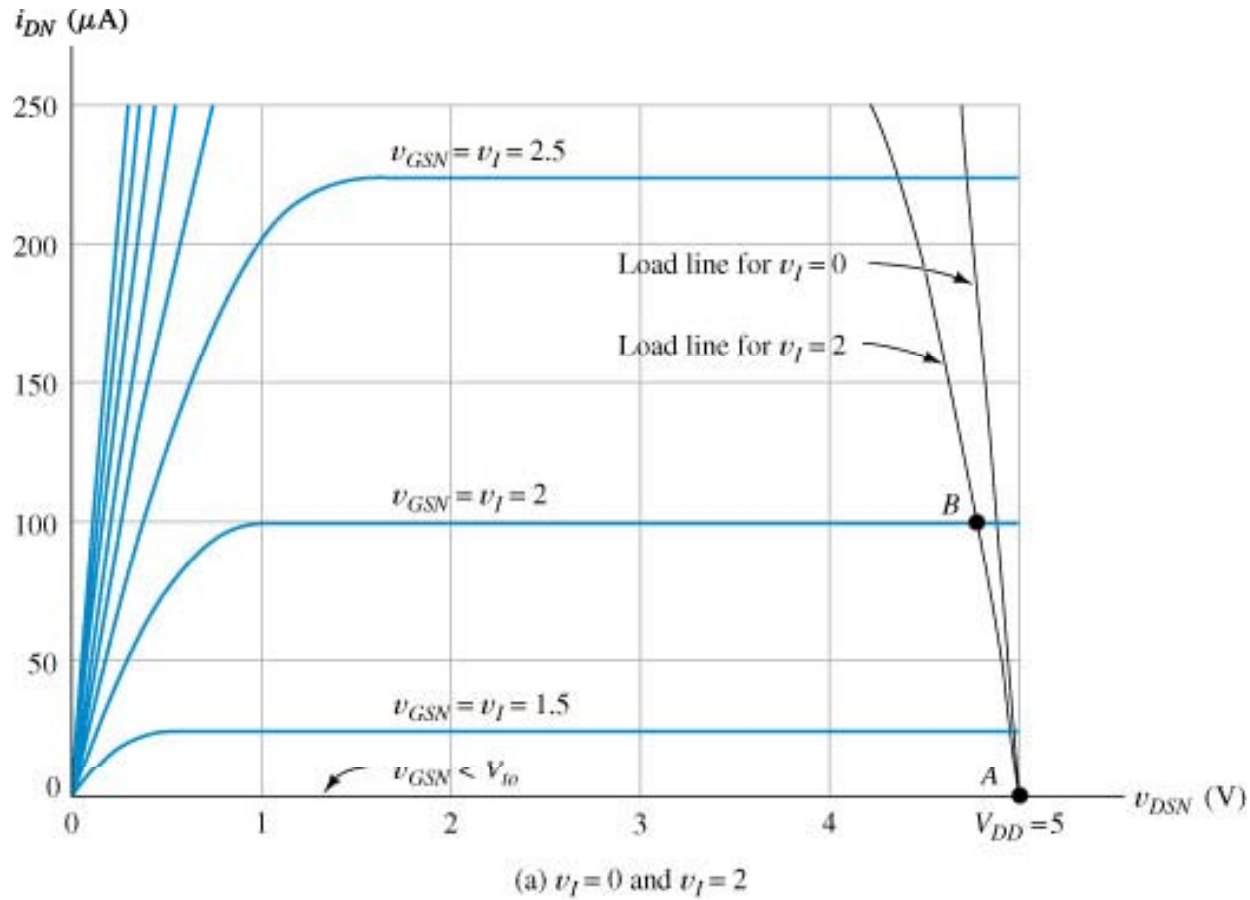


Figure 6.31a Graphical analysis of the CMOS inverter.

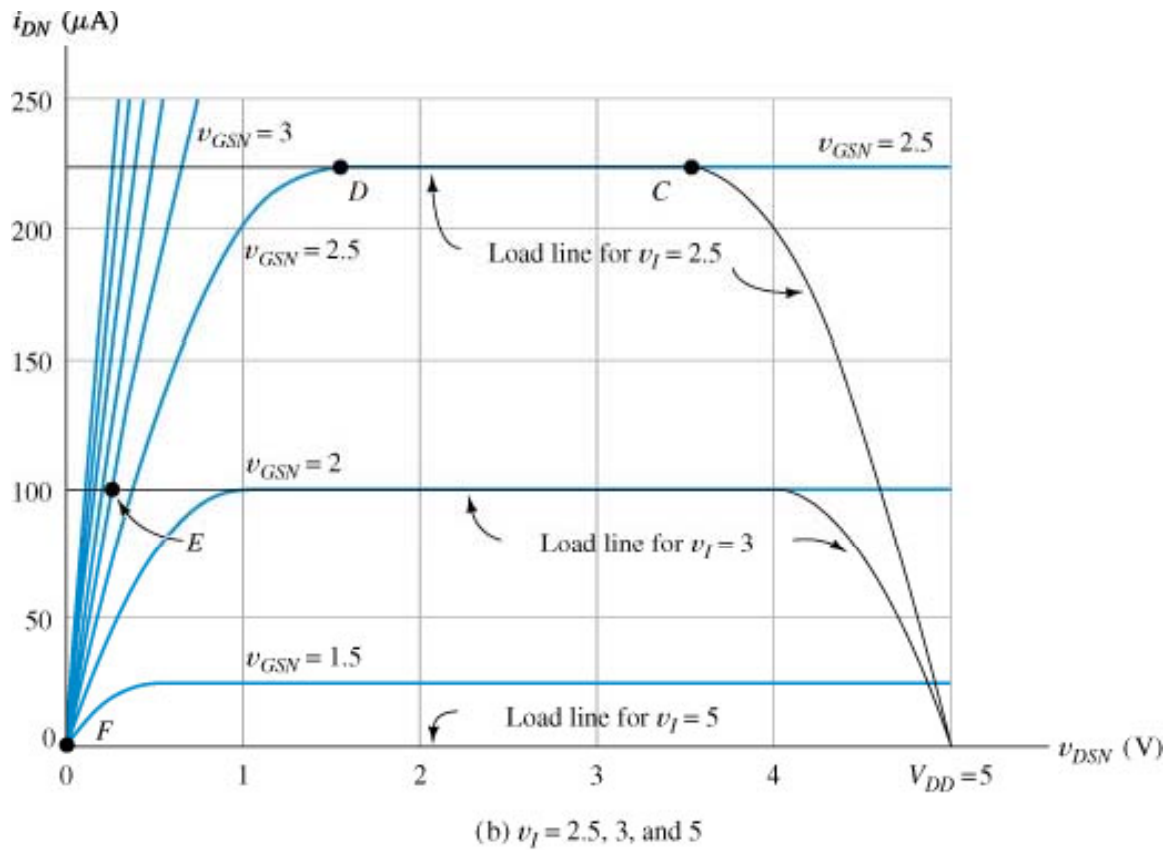


Figure 6.31b Graphical analysis of the CMOS inverter.

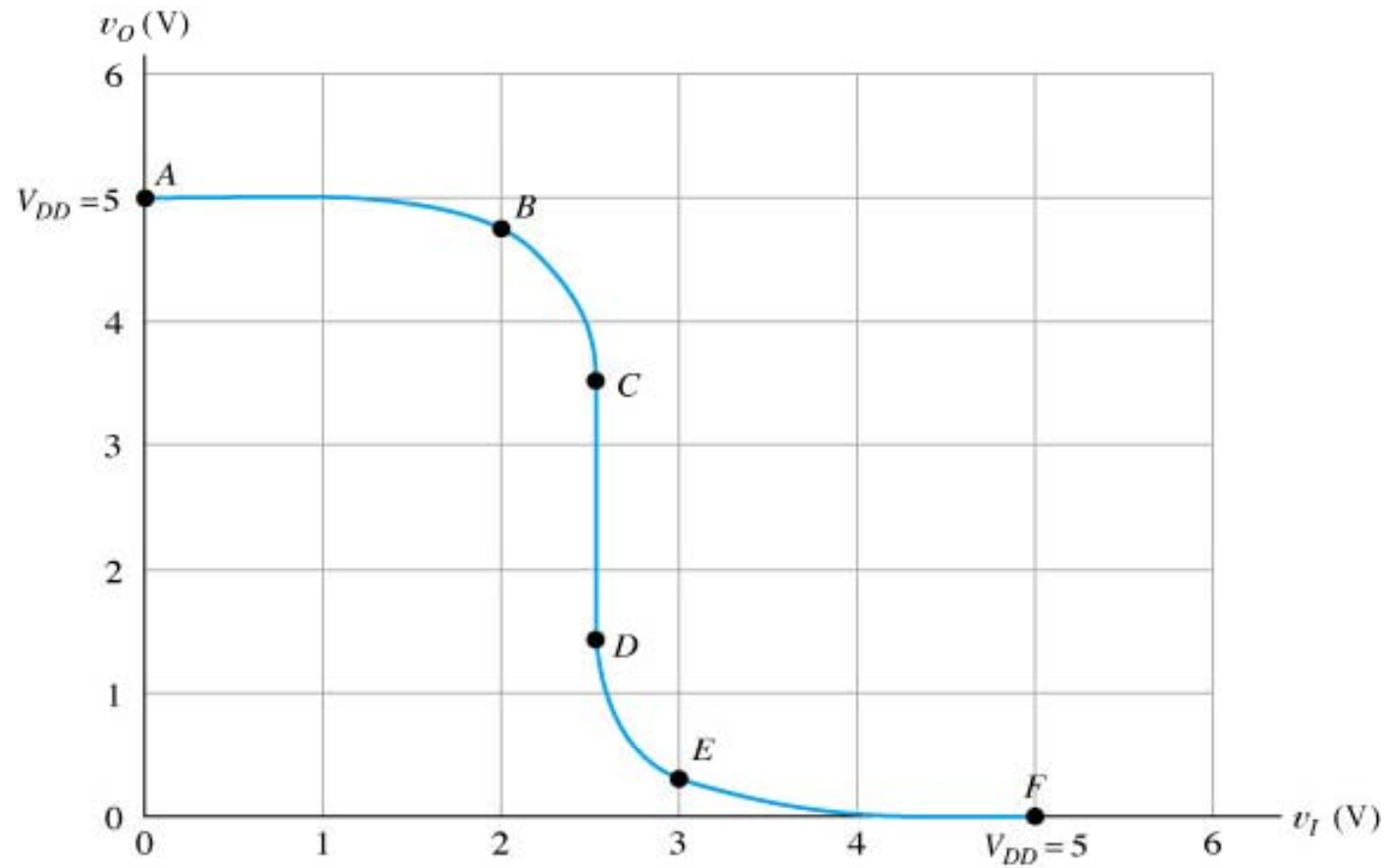


Figure 6.32 Transfer characteristic of a typical CMOS inverter.
The lettered points correspond to the points of Figure 6.31.

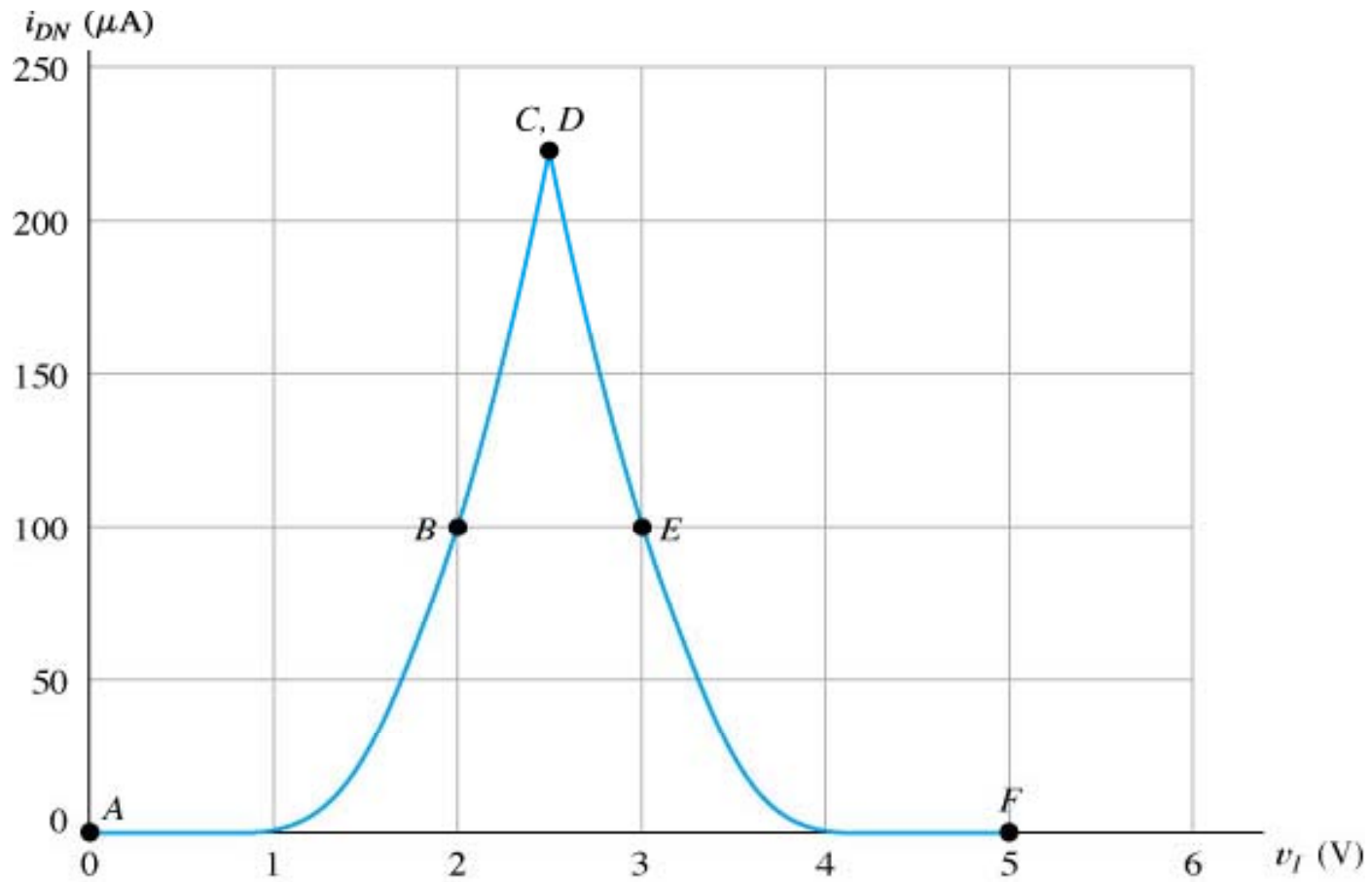


Figure 6.33 Supply current for a CMOS inverter.

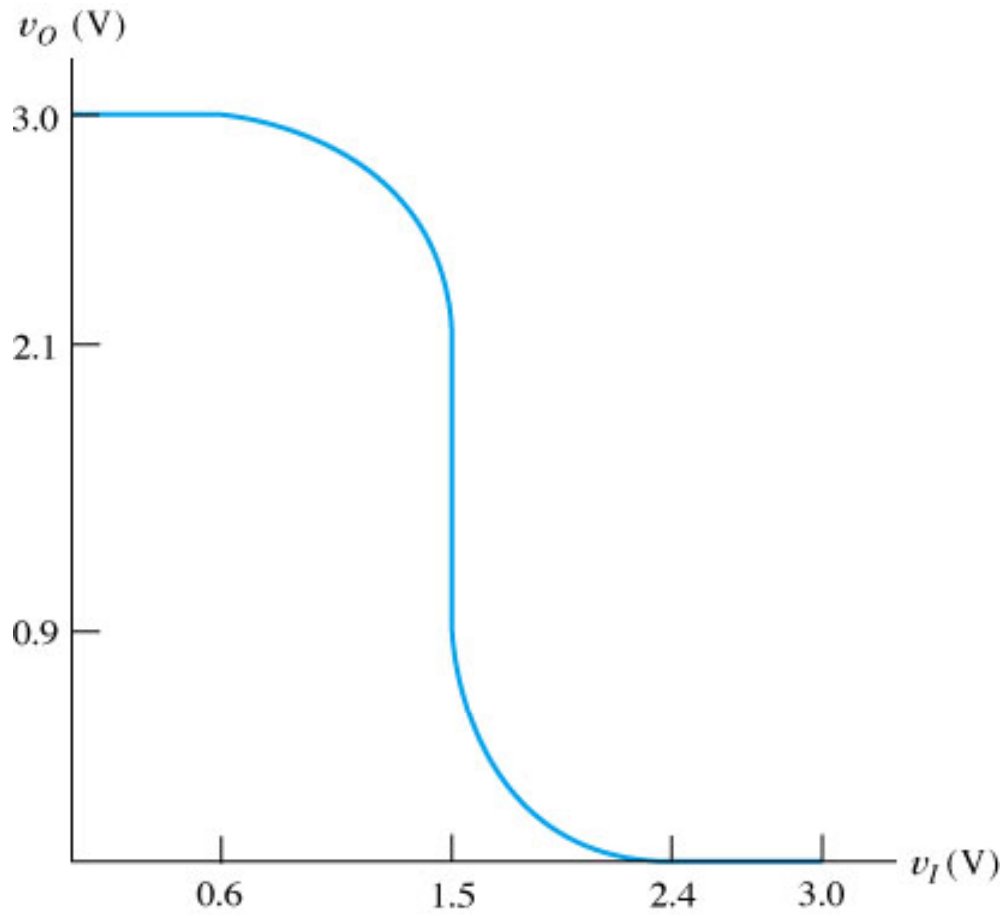


Figure 6.34 Transfer characteristic for CMOS inverter with $V_{ton} = 0.6$ V, $V_{top} = -0.6$ V, and $V_{DD} = 3$ V.

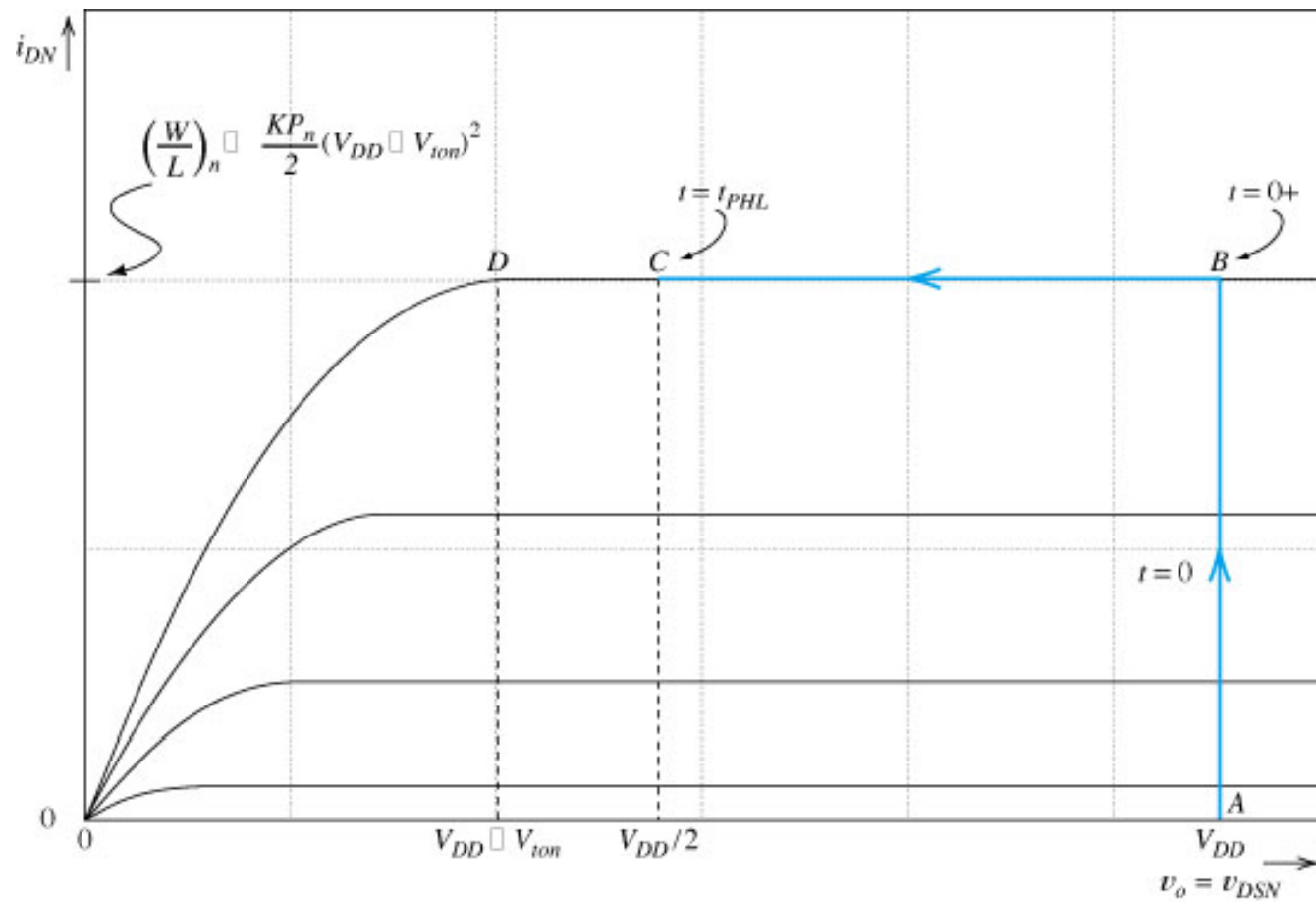


Figure 6.35 The high-to-low transition of the CMOS inverter.

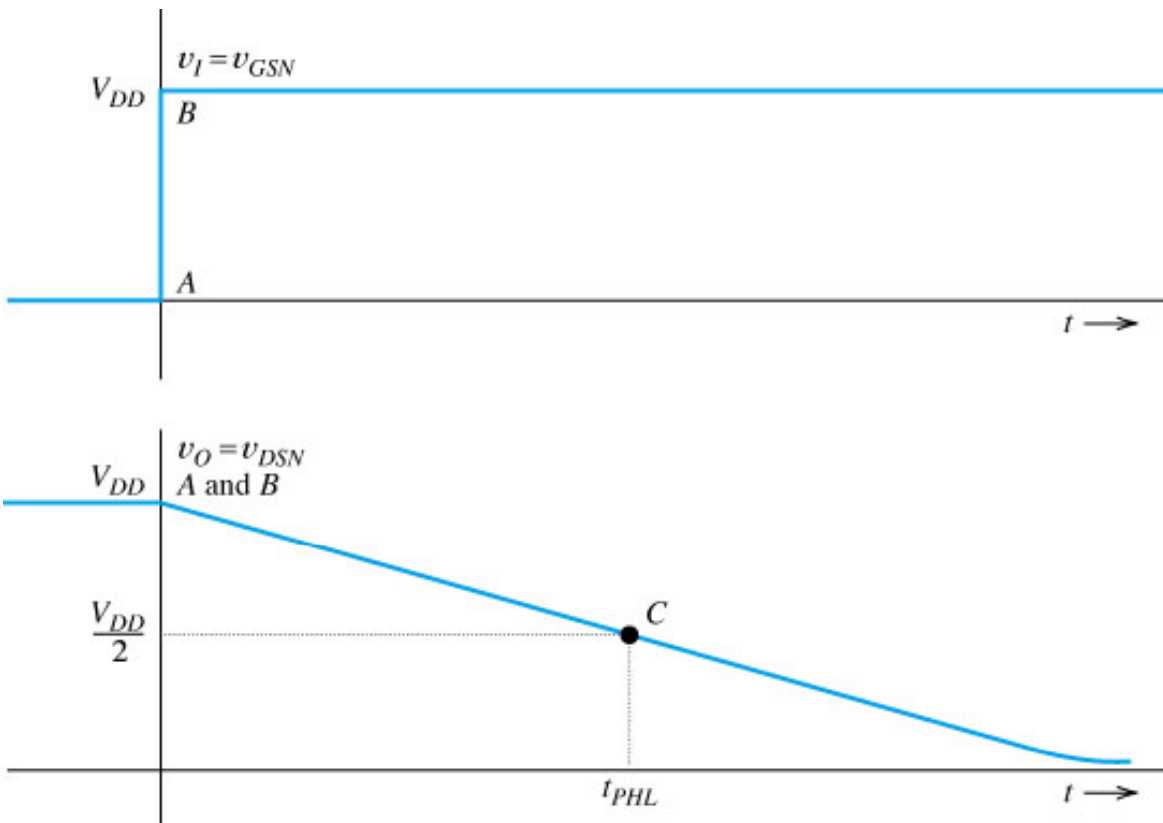


Figure 6.36 Idealized waveforms for the high-to-low transition of the CMOS inverter.

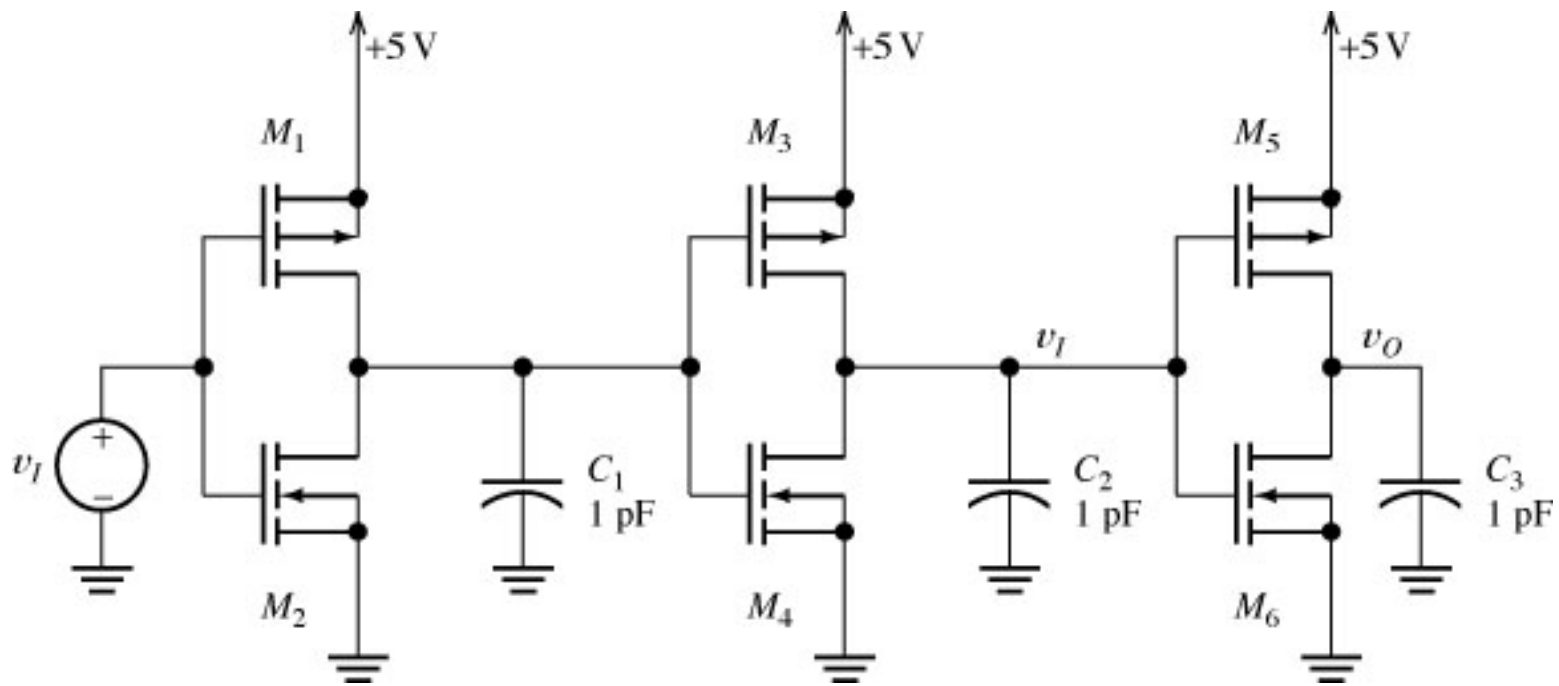


Figure 6.37 Cascade of three CMOS inverters.

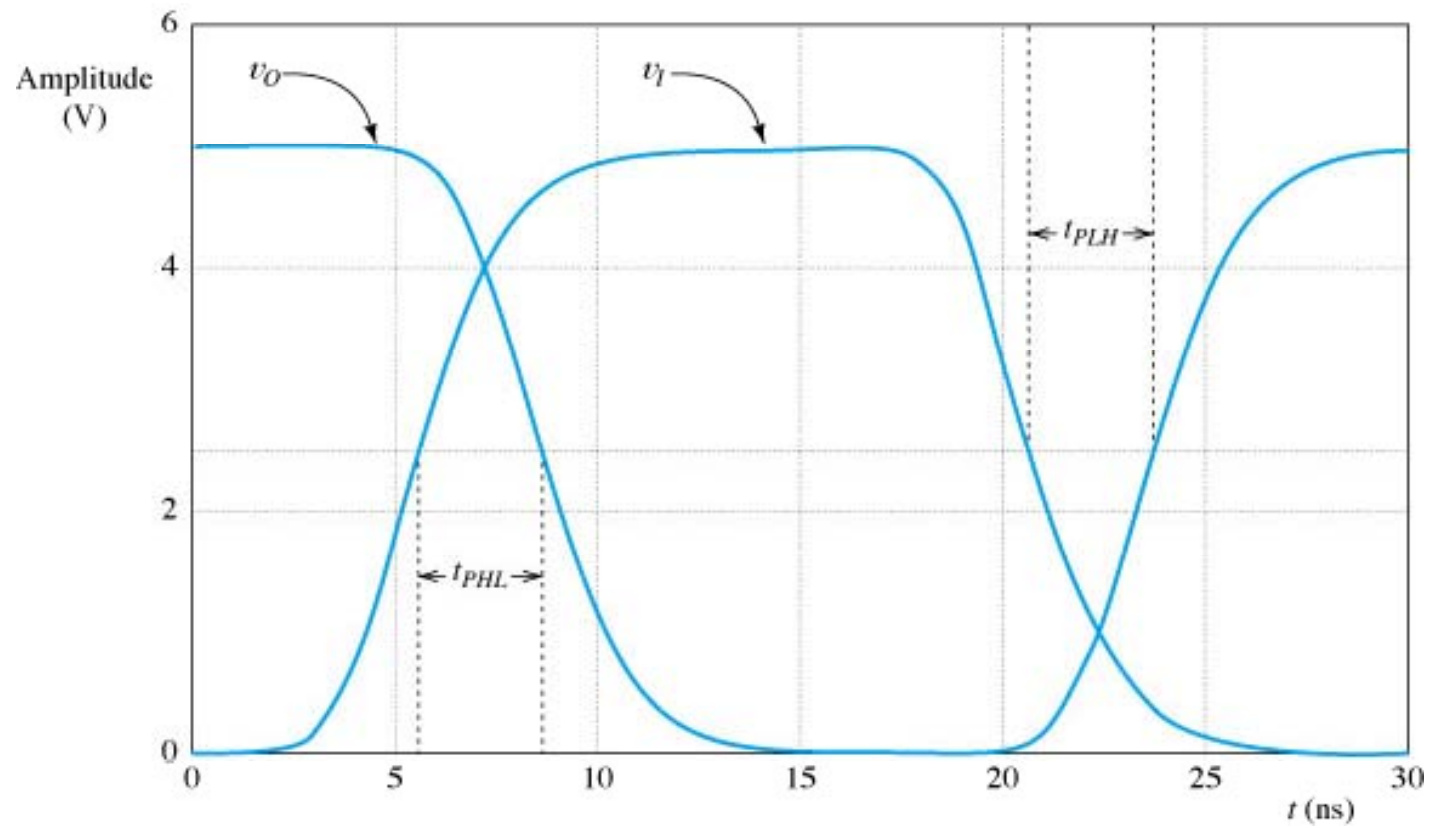


Figure 6.38 Waveforms for stage three of Figure 6.37.

Final Exam

- Monday, 5/11, 2 to 430 pm, 106 NH
- 6 or 7 questions (pages)
 - 3 questions on the last unit
 - Sections 5.1-5.7
 - Section 7.3
 - Sections 6.3 to 6.6
 - 3 questions on review
 - Sections 1.1 to 1.11
 - Sections 2.1 to 2.11
 - Sections 3.1 to 3.12
 - Chapter 4
 - Section 7.2
- Review old Tests and Quizzes (I will send email with links to old solutions.)

References and Endnotes

- Where not otherwise noted, figures with a figure number (e.g., Fig 3.2) are taken from:
 - Electronics, 2nd edition, by Allan R. Hambley, Prentice Hall, Upper Saddle River, NJ, © 2000.