

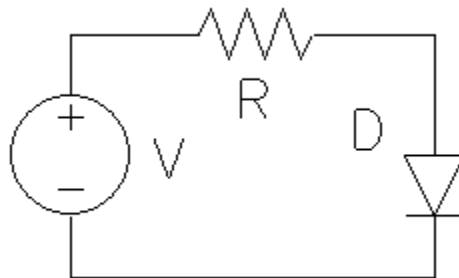
Project Assignment – Part 1 &2 (v 2.0)  
EE 2303/001 – Electronics I – Spring 2009  
Draft due 25 March 2009 – Final version due 15 April 2009  
<http://www.uta.edu/ronc/2303/project1.pdf>

All projects should be written on 8.5" x 11" paper with a cover sheet attached. The project report should be stapled only in the upper left-hand corner and no other cover or binder or folder should be used. The cover sheet should include (1) your name, (2) the project title, (3) the course name and number, and (4) your e-mail address. The report should include clearly marked sections on (a) purpose of the project and the theoretical background, (b) a narrative explaining how you did the project, (c) answers to all questions asked in the project assignment, and (d) a list of references used in the order cited in the report (the reference number should appear in the report each time the reference is used). All figures and tables should be clearly marked with a figure or table number and caption. The caption and labels on the figures should make the information in the figure comprehensible without reading further in the text of the report. Auxiliary information (such as SPICE data outputs, etc.) should be included in appropriate Appendices at the end of the report. Be sure to describe exactly how all results were obtained, giving enough information for anyone who understands EE 2303 to repeat your work. All work submitted must be original. If derived from another source, a full bibliographical citation must be given. (See all of the special notes on academic integrity – and those following – in the syllabus.)

### Part 1 Diode Load Line Quiescent Point: Comparison of the Iterative Solution to the PSpice Solution

**Purpose:** The purpose of this project will be to compare the solution for the load line quiescent point obtained by an iterative method with that obtained using PSpice.

The circuit used is shown in Figure 1. The diode current,  $i_D$ , is a function of the diode voltage,  $v_D$ , and is the simultaneous of two equations, the load-line equation and the Shockley equation for the diode.



**Figure 1.** The schematic diagram pertinent to this project. The diode current,  $i_D$ , is the current flowing in the diode in the direction of the arrow. The diode voltage,  $v_D$ , is the voltage drop across the diode.

The load line equation gives the relationship between the current,  $i_L$ , drawn from the ideal source,  $V$ , and the voltage drop,  $v_L (= V - i_L R)$ . Thus,

**Equation 1**  $i_L = (V - v_L)/R$

The Shockley equation gives the diode current,  $i_D$ , as a function of the diode voltage,  $v_D$ , with

**Equation 2**  $i_D = IS [\exp(v_D/(NV_t))-1]$ ,

where  $IS$  is the saturation current density,  $N$  is the ideality factor and  $V_t (= kT/q)$  is the thermal voltage ( $k$  is the Boltzman constant,  $T$  is the absolute temperature and  $q$  is the electron charge).

**Iteration:** To obtain the solution by iteration, each step consists of calculating the current by using Equation 1 (with the exception of step 1, where  $i_{L1} = V/(2R)$ ), and then calculating the voltage by noting that by the Kirchoff current law,  $i_L = i_D$ , and subsequently using Equation 2 in inverted format ( $v_D = NV_t \ln[(i_D/IS) + 1]$ ). Thus,

$$\text{Iteration 1: } i_{L1} = V/(2R) = i_{D1}, \text{ then } v_{D1} = NV_t \ln[(i_{D1}/IS) + 1]$$

$$\text{Iteration 2: } i_{L2} = (V - v_{D1})/R = i_{D2}, \text{ then } v_{D2} = NV_t \ln[(i_{D2}/IS) + 1]$$

$$\text{Iteration 3: } i_{L3} = (V - v_{D2})/R = i_{D3}, \text{ then } v_{D3} = NV_t \ln[(i_{D3}/IS) + 1]$$

...]

$$\text{Iteration n: } i_{Ln} = (V - v_{D(n-1)})/R = i_{Dn}, \text{ then } v_{Dn} = NV_t \ln[(i_{Dn}/IS) + 1]$$

The iteration process is usually continued until the differential error ratio,  $\Delta$ ,

$$\text{Equation 3} \quad \Delta \equiv |i_{Dn} - i_{D(n-1)}|/i_{Dn}$$

is less than some predetermined fractional difference (i.e., 1%, etc.).

**Obtaining the PSpice solution:** First, the solutions cannot be compared unless the same value for  $V_t$  is used. The value to be used throughout the entire project is  $V_t = 25.852$  mV.

**Question 1.** (a) Verify from the Shockley equation that when an independent current source drives a current of  $i_D = IS(\exp(1) - 1)$ , the voltage measured across the diode should be  $NV_t$ . (b) What is the temperature in C which corresponds to  $V_t = 25.852$  mV?

**Question 2.** Using a circuit as defined in Question 1(a), determine the values that should be used for the PSpice Analysis/Setup/Option parameters, GMIN, NUMDGT, and TNOM in order for the value of  $V_t = 25.852$  mV to at least 5 significant figures for the diode defined in Question 3.

**Question 3.** Given that  $IS = 8.5E-13$ ,  $N = 1.18$ ,  $V = 2.7$  Volts, and  $R = 0.10, 0.27, 1.0, 2.7, 10, 27, 100, 270,$  and  $1,000$  Ohms, use PSpice to determine the quiescent point values for  $i_{DQ}$  and  $v_{DQ}$  corresponding to each  $R$  value given. Report your results in the form of a table with column headings  $R$ ,  $i_{DQ}$  and  $v_{DQ}$  and a row for each of the values of  $R$  given above. Be sure the number of significant figures reported for  $i_{DQ}$  is commensurate with 5 significant figures for  $v_{DQ}$  as is appropriate from Question 2 above.

### Obtaining the Iterated Solutions:

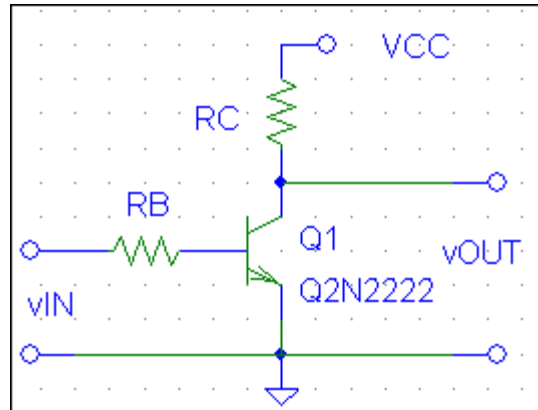
**Question 4.** Using the iterative procedure defined above to determine the quiescent point values for the same circuit parameters defined in Question 3. Perform the iterative procedures in each case until the value of  $\Delta$  is  $\leq 1\%$ . Report your 1% results in the form of a table with column headings  $R$ ,  $i_{DQ,1\%}$  and  $v_{DQ,1\%}$  and a row for each of the values of  $R$  given above. Be sure the number of significant figures reported for  $i_{DQ}$  is commensurate with 5 significant figures for  $v_{DQ}$  as is appropriate from Question 2.

**Question 5.** Compare the PSpice and iterative results by calculating the relative difference,  $r$ , between the PSpice-calculated current,  $i_{DQ}$ , and the iterative solution,  $i_{DQ,1\%}$  ( $r = |i_{DQ} - i_{DQ,1\%}|/i_{DQ}$ ). Tabulate the  $r$  values for each value of  $R$  given in 3. Comment on the magnitude of  $r$ , and any trends observed.

## Part 2 BJT Inverter Design and Optimization: Comparison of the Basic Optimized Design to the PSpice Solution and Optimization

**Purpose:** The purpose of this project will be design a basic BJT inverter to certain specifications, compare the design to the PSpice simulation, and optimize the performance in PSpice.

The circuit to be used for the inverter is shown in Figure 2. The BJT to be used is the 2N2222. A supply voltage, VCC, will be decided as well as values for the circuit elements RC and RB. This will be done in a



**Figure 2.** The basic BJT inverter topology.

manner such that the gain,  $G = \Delta v_{OUT} / \Delta v_{IN}$ , the range of values for  $v_{IN}$ , the range of values for  $v_{OUT}$  maximize the Figure of Merit (FOM) function given in Equation 3.

**Equation 3** 
$$FOM = \{|G| \times |\Delta v_{OUT}| \times |\Delta v_{IN}|\} / \{|G_{max}| \times |\Delta v_{OUTmax}| \times |\Delta v_{INmax}|\},$$

where  $\Delta v_{OUT} = v_{OUTcutoff} - v_{OUTsaturation}$ , and  $\Delta v_{IN} = v_{INsaturation} - v_{INcutoff}$ . This should simultaneously give maximum gain and range of input and output. The design will choose the optimum value of RC, RB and VCC, keeping in mind the parameters for the 2N2222 as given on the Fairchild website. Special attention should be given to the maximum CE voltage, the maximum BE voltage, and the maximum power the 2N2222 is rated for. A criterion for the transition from forward active to saturation will need to be defined as well as a criterion for the forward active to cutoff.

**2a.** First, assume the source,  $v_{IN}$ , has zero source resistance and the output,  $v_{OUT}$  is looking into an open circuit. Develop and describe in detail the process used to determine RC, RB and VCC. Simulate the same circuit in PSpice, and compare the result in simulation to the hand-calculated derivation done for G, and FOM.

**2b.** Next, assume the source,  $v_{IN}$ , has 1 k $\Omega$  source resistance and the output,  $v_{OUT}$  is looking into a 1 k $\Omega$  resistance. Develop and describe in detail the process used to determine RC, RB and VCC. Simulate the same circuit in PSpice, and compare the result in simulation to the hand-calculated derivation done for G, and FOM.