Project 1 Assignment – Diode Characterization *(Draft)*

EE 5342 - Semiconductor Device Theory

Project 1 Test on March 24, 2005

Download this assignment at http://www.uta.edu/ronc/5342/projects/5342Project1.pdf

All project solutions should be submitted on 8.5" x 11" paper with a cover sheet attached when the Project 1 Test is taken. The project report should be limited to 20 pages and stapled only in the upper left-hand corner with no other cover or binder or folder. The cover sheet should include (1) your name, (2) the project title, (3) the course name and number, and (4) your e-mail address. The report should include clearly marked sections on (a) purpose of the project and the theoretical background, (b) a narrative explaining how you did the project, (c) answers to all questions asked in the project assignment, and (d) a list of references used in the order cited in the report (the reference number should appear in the report each time the reference is used). All figures and tables should be clearly marked with a figure or table number and caption. The caption and labels on the figures should make the information in the figure comprehensible without reading further in the text of the report. Auxiliary information (such as SPICE data outputs, etc.) should be included in appropriate Appendices at the end of the report. Be sure to describe exactly how all results were obtained, giving enough information for anyone who understands EE 5342 to repeat your work. All work submitted must be original. If derived from another source, a full bibliographical citation must be given. (See all of Notes 5 and 6 in the syllabus.) Download a sample solution at http://www.uta.edu/ronc/5340/project/40ProjectSolution03.pdf.

I. Semiconductor Device Capacitance-Voltage Characteristics

A. The Capacitance-Voltage (C-V) characteristics of a semiconductor device are given in http://www.uta.edu/ronc/5342/projects/Project_1/CVdata.xls

Fit the SPICE model equation given in Equation 1 to the data in order to determine the values for CJ0, VJ and M.

$$C_j = CJ0\left[1 - \frac{V_a}{VJ}\right]^{-M} \qquad \textbf{Equation 1}$$

A1. Develop extraction techniques on the data given in the Excel file for determining CJ0, VJ and M. You might want to do this along the lines of Lecture 10, page 9 and following.

A2. Include a table of the C-V data, including columns for $y \equiv \{d[\ln(CJ)]/dV\}^{-1}$, and dy/dV. Also include a graph of y vs. V. Refer to the table to form a hypothesis for the best range of data to use for the SPICE capacitance model equation.

A3. Use these extraction techniques on the data given to determine estimates for CJO, VJ and M. What forward voltage range actually fits the standard CV model? (Hint: You might want to try to prove that this will be for Va > VPT.)

A4. Using the pin/srd diode theory, determine the punch through voltage, V_{PT}, for this device.

A5. Determine the thickness of the intrinsic region from the CV data.

A6. What adjustments to the SPICE model can you suggest in order to create a better model? (Hint: What auxiliary circuit would you add in order to model the diode for operation at Va < VPT?)

B. A7. Add a column to the table generated in part A2 which includes the values calculated with the extracted model parameters in Equation 1. Determine the least squares error (L.S.E.) between the data and the model equation and comment on the consequence of this error.

$$L.S.E. = \sum \sqrt{(C_{SPICE}(v_i))^2 - (C_{data}(v_i))^2} \Big/ (\#\text{ data points}) \qquad \textbf{Equation 2}$$

C. If the area of this junction is known to be 804 sq. microns, determine the doping concentration on the lightly doped side as a function of depletion width. The concentration is related to the C-V data by Equation 3.

$$N(x_n) = -\frac{2}{\varepsilon q A^2 \frac{d(C^{-2})}{dV}} \qquad \textbf{Equation 3}$$

C1. Plot N(x) as a function x_n. Consider data for -5.0 < va < 0.5 V. What doping function $N(x_n)$ best fits this plot (linear, square, exponential, etc.)?

C2. Is the function determined in C1 consistent with the value of M determined in A2? Why, and should a different model be used in SPICE for this diode?

II. Semiconductor Device Static Diode Characteristics

D. See http://www.uta.edu/ronc/5342/projects/Project_1/IVdata.xls for the IV data.

D1. Use these data to extract values for IS, N, ISR, NR, and RS. Document the procedures you use and why you choose these procedures.

D2. Develop the best least squares static model values for IS, N, ISR, NR, and RS for operating the diode in the range 700mV < vext < 1000mV. (i.e. minimize the least squares error – by trial and error)

$$L.S.E. = \sum \sqrt{(i_{SPICE}(v_i))^2 - (i_{data}(v_i))^2} \Big/ (\#\text{ data points}) \qquad \textbf{Equation 4}$$

D3. Repeat D2 for the range 300mV to 1V.

D4. Comment on the differences in the parameter values obtained in D2 and D3.

III. Semiconductor Device Y-parameters

E. See http://www.uta.edu/ronc/5342/projects/Project_1/Ydata.xls for the Y-parameter data.

E1. Use the corner frequencies at each voltage to determine the TT parameter and the C(Va) function over the range of Va values given.

E2. Make a comparison of the various limiting values of the Y-parameter data to the values you observe from the static parameters obtained in part D. For instance, the low frequency limit of Re(Z) should be

$$\lim_{f \to 0} Re\{Z\} = g_d^{-1} + RS \qquad \textbf{Equation 5}$$

The high frequency limit should be RS.

E3. Is the value of gd obtained for each Vd in part E2 consistent with the IV data and the N value you obtained? Comment on any differences.

E4. Confirm your determination of IS, N, ISR, NR and RS based on these Y-parameters.

E5. This data will not fit the ordinary diode model exactly. Is it possible to make a combination of diodes that will fit the data better? Describe.

Note 1: The Re{Z} IS NOT the same as 1/Re{Y}. Re{Z} = Re{1/Y} = Re{1/(Re{Y}+j*Im{Y})}