

# EE 5342, Spring 2005

## Semiconductor Device Modeling and Characterization

(View at <http://www.uta.edu/ronc/5342/syllabus.htm>, download at <http://www.uta.edu/ronc/5342/syllabus.pdf>)

**Instructor:** Professor R. L. Carter, [ronc@uta.edu](mailto:ronc@uta.edu), <http://www.uta.edu/ronc>, 524 Nedderman, (office hours: <http://www.uta.edu/ronc/schedule/>), 817/273-3466, fax 817/272-2253.

**GTAs:** Mr. Zheng Li, [zxl6576@exchange.uta.edu](mailto:zxl6576@exchange.uta.edu), 2:30PM to 5:30PM, o/h: 249 ELB Tuesday and Thursday.

**Course Learning Goals and Objectives:** To model and characterize integrated circuit structures and devices using SPICE and SPICE-like descriptions of the devices.

**Class Meetings:** Tues/Thur, 9:30 to 10:50 AM, 105 Nedderman Hall.

**Attendance Policy:** Attendance at every class session for the entire 80-minute period is strongly advised.

There will be no videotapes of the lectures available. Drafts of the lectures in \*.ppt format will be posted by 4 PM the day before class at <http://www.uta.edu/ronc/5342/lectures>. Bring a copy to class.

**Use of e-mail:** Sign up for the EE 5342 list. To subscribe, send mail to [listserv@listserv.uta.edu](mailto:listserv@listserv.uta.edu) with the command (paste it without quotes) "subscribe EE5342" in the message. List subscribers will receive all messages sent to the class. Send questions to [ronc@uta.edu](mailto:ronc@uta.edu) with "EE 5342" included in the subject line.

**Workstation Labs:** The SunSolaris (Gamma2 – ELB 212) system is set up with IC-CAP™.

**Text** (On reserve in the Science and Engineering Library): *Semiconductor Device Modeling with SPICE, 2nd ed.*, by Paolo Antognetti and Giuseppe Massobrio, McGraw-Hill, New York, 1993, ISBN 0071349553 (paperback) or 007 0024693 (hardback). Listed as T in the assignments.

**Device Characterization References:** (On reserve in the Science and Engineering Library):

- *Introduction to Device Modeling and Circuit Simulation*, by Tor A. Fjeldly, Trond Ytterdal, and Michael Shur, John Wiley and Sons, New York, 1998.
- *Semiconductor Material and Device Characterization*, by Dieter K. Schroder, John Wiley and Sons, New York, 1990. Listed as S in the assignments. This text emphasizes primarily material characterization, so select device modeling topics primarily.

**Spice References:** (Books on reserve in the Science and Engineering Library are marked<sup>R</sup>.)

- <sup>R</sup>*MicroSim PSpice for Windows, 2nd ed*, by Goody, Prentice-Hall, Upper Saddle River, N.J., ©1998.
- <sup>R</sup>*Computer-Aided Circuit Analysis Using PSpice* by Walter Banzhaf, Regents/Prentice Hall, Englewood Cliffs, NJ, ©1992
- <sup>R</sup>SPICE: A Guide to Circuit Simulation and Analysis Using PSpice, 3rd ed., by Paul W. Tuinenga, Prentice Hall, Englewood Cliffs, NJ, ©1995.
- *Schematic Capture with MicroSim Pspice: for Windows 3.1, 4<sup>th</sup> Ed.*, by Herniter, ©2000, Prentice-Hall
- PSpice™ is available by download from [Orcad](http://www.orcad.com) or from the UTA HKN chapter chapter at <http://hkn.uta.edu>.
- Prof. Dillon's excellent tutorial for PSpice™ is at <http://rock.uta.edu/dillon/pspice/>

**Device Electronics References:** (On reserve in the Science and Engineering Library)

- *Device Electronics for Integrated Circuits*, 3rd ed., by Richard S. Muller, Theodore I. Kamins, and Mansun Chan, John Wiley and Sons, New York, 2003. ISBN: 0-471-59398-2. Listed as D in the assignments.
- *Devices for Integrated Circuits : Silicon and III-V Compound Semiconductors*, by H. Craig Casey, John Wiley, New York, 1999. Listed as DI in the assignments.

**Projects, Tests and Grading Formula** (Sample tests are posted at <http://www.uta.edu/ronc/5342/tests/>):

- 60% total for projects (see syllabus for due dates for each project – 30% each for P1 (3/10) and P2 (5/14) – These dates are when a test on the project will be given and the due dates for the project to be turned in.)
- 20% total, one mid-term (MT – February 10)
- 20% for final (FN – May 12 – required)

i.e., the grade will be computed from the formula,  $Grade = (P1 + P2)*0.3 + (MT + FN)*0.2$

**Grading Scale:**

- A = 90 and above
- B = 75 to 89
- C = 60 to 74
- D = 50 to 59
- F = 49 and below

**Project Assignments:** Project assignments will be posted at <http://www.uta.edu/ronc/5342/projects>. A device of the student's choice may be substituted for one of the assigned projects by arrangement with the instructor. Project format and written content will be discussed and will be included in the grade.

(Lecture notes, when published, are at <http://www.uta.edu/ronc/5342/lectures>)

CL	DATE	DAY	P/T	STUDY ASSIGNMENTS
1	18-Jan-05	T		<b>Semiconductor Electronics Review</b>
2	20-Jan-05	Th		T(Appendix A.1), D(Ch 1)
3	25-Jan-05	T		DI(Chs 2&3), S(Chs 1 & 2)
4	27-Jan-05	Th		
5	01-Feb-05	T		<b>P-N and Schottky diodes, and contacts Census 2/2</b>
6	03-Feb-05	Th		T(Appendix A.2, Ch 1 and Appendix C); D(Ch 3, 4 and 5)
7	08-Feb-05	T		DI(Chs 4, 5 & 6), S(Chs 3 & 4.1-4.3)
8	10-Feb-05	Th	MT	
9	15-Feb-05	T		
10	17-Feb-05	Th		
11	22-Feb-05	T		<b>Bipolar junction transistors</b>
12	24-Feb-05	Th		T(Chs 2 & 5); D(Ch 6 & 7)
13	01-Mar-05	T		DI(Ch 9), S(Chs 4 & 5)
14	03-Mar-05	Th		
15	08-Mar-05	T		
16	10-Mar-05	Th	P1	Project due and in-class exam on project
17	22-Mar-05	T		<b>Spring Vacation 3/14 to 3/20</b>
18	24-Mar-05	Th		
19	29-Mar-05	T		<b>MOSFETs</b>
20	31-Mar-05	Th		T(Chs 4 & 6); D(Ch 8, 9 & 10)
21	05-Apr-05	T		DI(Chs 7 & 8), S(Chs 4.6, 5.3 & 6)
22	07-Apr-05	Th		
23	12-Apr-05	T		<b>Last day to drop class, April 15</b>
24	14-Apr-05	Th	P2	Project due and in-class exam on project
25	19-Apr-05	T		
26	21-Apr-05	Th		
27	26-Apr-05	T		
28	28-Apr-05	Th		<b>MESFETs, HEMTs and HBTs</b>
29	03-May-05	T		T(Ch 9.1); D(Ch 4.5)
30	05-May-05	Th		DI(Chs 5.6.4, 6.7, 6.8, and 9.9), S(Ch 4.7)
31	12-May-05	Th	FN	8 to 1030 AM, Grades due 5/17, Summer Term begins 05/31

**Notes:**

1. This syllabus may be changed by the instructor as needed for good academic practice. Use the "refresh" or "reload" function on your browser.
2. Quizzes and tests are open book (must have a legally obtained copy-no Xerox copies). Calculator allowed.
3. There will be no make-up, or early exams given. Attendance is required for all tests.
4. Americans with Disabilities Act: The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 93112—The Rehabilitation Act of 1973 as amended. With the passage of new federal legislation entitled Americans with Disabilities Act – (ADA), pursuant to section 504 of The Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens. As a faculty member, I am required by law to provide “reasonable accommodation” to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with informing faculty at the beginning of the semester and in providing authorized documentation through designated administrative channels. In conformance with the Americans with disabilities Act, I state that, "If you require an accommodation based on disability, I would like to meet with you in the privacy of my office during the first week of the semester to make sure you are properly accommodated. Contact Mr. Jim Hayes (272-3364) for Information."
5. It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University. "Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, submission for credit of any work or materials that are attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts." (Regents' Rules and Regulations, Part One, Chapter VI, Section 3, Subsection 3.2, Subdivision 3.22). ANY CHEATING WILL RESULT IN SEVERE PENALTIES. All work submitted must be original. If from another source, a full bibliographical citation must be given. See <http://www.uta.edu/studentaffairs/judicialaffairs/> for UTA policies.
6. **By EE Dept policy, sign and submit the document at <http://www.uta.edu/ronc/5342/Ethics.htm> to Prof. Carter.**
7. If identical papers are submitted by different students, the grade earned will be divided among all identical papers.
8. A paper submitted for regrading will be compared to a copy of the original paper. If changed, points will be deducted.