Project 3 Test 4 - EE 5342 (print last name) ______________________ (print first name) _____________________
8:00 to 10:30 AM, Thursday May 13, 2004, 105 Nedderman Hall
80 minutes allowed (last four digits of your student #) _____________ (e-mail _if_ new)______________________

Instructions: Seat Number ____________

1. Do your own work. DO NOT REMOVE THE STAPLE ON THIS EXAM.
2. You may use a legal copy of the text by Massobrio and Antognetti. You may write notes in your text. You may NOT pass a book or note sheet to another student, or class notes or previously solved problems. **You may use your Project 1 solution and must submit it with this test in your exam packet**.
3. Calculator allowed. You may NOT share a calculator with another student.
4. Where values or equations are given on this cover sheet, use them in lieu of any other source. If a value is not given, explicitly state definitions and assumptions that you use.
5. Where possible, calculate parameters rather than read them from a graph.
6. Do all work in the spaces provided on this exam paper. If you write on the back of a sheet, make the notation "PTO" in your solution in order to assure that material written on the back of the page is evaluated for a grade. AN EXTRA BLANK SHEET IS ATTACHED AT THE BACK OF THE EXAM.
7. Show all calculations, making numerical substitutions and giving numerical results where possible.
8. **The total for the test is 75. Up to 25 additional points will be given for the Project report**.
9. Unless stated otherwise,
   $T = 300K$, $V_t = 25.852$ mV
10. Unless otherwise stated, the material is silicon (300K) with
    $n_i = 1.45E10\ cm^{-3}$ $N_c = 2.8E19\ cm^{-3}$ $q\chi_{Si} = 4.05$ eV
    $E_{g,Si} = 1.124$ eV. $N_v = 1.04E19\ cm^{-3}$
11. For the work function of poly silicon, use $\phi_{n+} = \chi_{si} = 4.05$ V
    $\phi_{p+} = \chi_{Si} + E_{g,Si}/q = 5.174$ V.
12. For minority carrier (either electrons or holes) lifetime in silicon, use the relationship
    $\tau_{min} = (4.5E\text{-}5\ sec)/(1 + N_i/1E17 + (N_i/5E17)^2)$,
    where N_i = the total impurity concentration in cm^{-3}
13. For holes in silicon doped <u>primarily</u> with boron*, assume
    $\mu_p = \{470.5\div[1+(N_i\div 2.23E17)^{0.719}]\}+44.9$, in cm^2/V-sec.
14. For electrons in silicon doped <u>primarily</u> with phosphorous*, assume
    $\mu_n = \{1414\div[1+(N_i\div 9.2E16)^{0.711}]\}+68.5$, in cm^2/V-sec.
15. For electrons in silicon doped <u>primarily</u> with arsenic, assume
    $\mu_n = \{1417\div[1+(N_i\div 9.68E16)^{0.68}]\}+52.2$, in cm^2/V-sec.
    (In 12 through 15, N_i = the total impurity concentration in n- or p-type material, compensated or not.)
    (*13 may be used as an approximation for holes as minority carriers, likewise *14 for minority electrons.)
16. Metal gate work functions should be assumed to be
    $\phi_{M,Al} = 4.1$ V for aluminum, $\phi_{M,Pt} = 5.3$ V for platinum, $\phi_{M,Au} = 4.75$ V for gold
17. The electron affinity of SiO_2 is $\chi_{SiO2} = 1.00$ V.
18. Planck constant $h = 6.625E\text{-}34$ J-s = 4.135E-15 eV-s, (1 eV = 1.602E-19 Joule).
19. free electron mass $m_o = 9.11E\text{-}28$ g.
20. Boltzmann constant, $k = 1.38066E\text{-}23$ J/K
21. Electron charge, $q = 1.60218E\text{-}19$ Coulomb
22. Permittivity of free space, $\varepsilon_o = 8.854E\text{-}14$ Fd/cm
23. Relative permittivity of silicon, $\varepsilon_r = 11.7$
24. Relative permittivity of silicon dioxide, $\varepsilon_{rOx} = 3.9$
25. The breakdown voltage of an abrupt (step) junction (asymmetrical or one-sided) diode with doping on the lightly doped side of N_B is $V_B = 60(Eg/1.1)^{3/2}\ (10^{16}/N_B)^{3/4}$ V. The critical field for breakdown is modeled as $E_{crit} = (120V\cdot qN_B/(\varepsilon_r\varepsilon_0))^{1/2}\cdot(Eg/1.1)^{3/4}\cdot(10^{16}/N_B)^{3/8}$
26. Each part is worth [x] points, as given in the problem.

In the small-signal model of the CMOS transistors, the output resistance, $r_o = r_d$, is defined as $r_o = \frac{\partial V_{DS}}{\partial I_D}$

1. [15] Assume the device is in the saturation region, the Shichman and Hodges (simple square-law) model applies, and neglecting the channel-length modulation effect, what is the r_o value?

   Because $I_D = \frac{1}{2} m_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$, $r_o = \infty$

2. [20] If channel-length modulation is taken into account, show that r_o is approximately $1/(\lambda I_D)$, where l is the channel-length modulation coefficient and I_D is the drain current.

   For an NMOS transistor, $I_D = \frac{1}{2} m_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + l V_{DS})$

   Taking the differential on both sides, we get

   $$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2} m_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot l$$

   if the variation of I_D caused by the channel-length modulation effect is small ($\lambda V_{DS} << 1$), we have

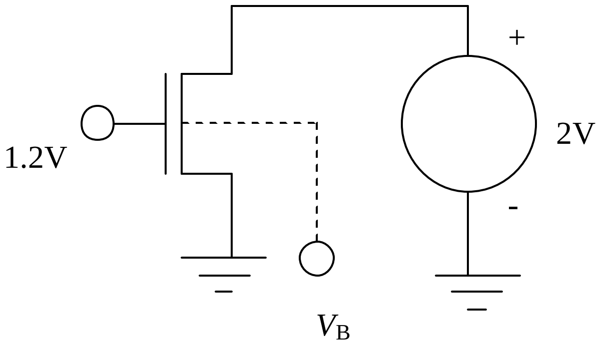
   $$\frac{\partial I_D}{\partial V_{DS}} \approx I_D \cdot l$$

   so, $r_o = \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{l I_D}$

3. [10] Which effect in the BJT device characteristics corresponds to the channel-length modulation effect in CMOS device?

   The Early effect.

4. [20] For the circuit in the following figure, *sketch* the drain current if the bulk voltage, V_B, varies from $-\infty$ to 0. Assume V_{TH0}=0.6V, $g = 0.4\text{V}^{1/2}$, $2F_F = 0.7$V and $m_n C_{ox}(W/L) = 2\times10^{-3}$ A/V^2. Mark key point(s) on the plot.



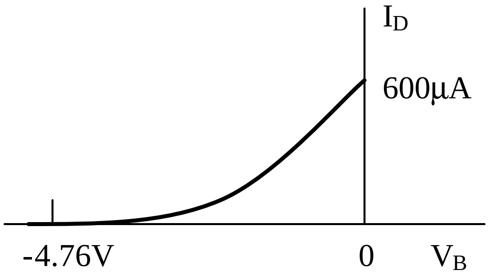
If V_B is too negative, the threshold voltage will exceeds 1.2V. In this case, the device is off and the drain current is 0. The bulk voltage that makes the threshold voltage equal to 1.2V can be calculated as:

$$1.2 = 0.6 + 0.4 \cdot (\sqrt{0.7 - V_B} - \sqrt{0.7})$$

we get V_B=-4.76V.

If $-4.76<V_B<0$, $V_{DS}>V_{GS}-V_{TH}$ ➔ Device is saturated

Therefore, the current increases according to $I_D = \frac{1}{2} m_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})^2$ in this region. Finally, the drain current is 600μA at $V_B=0$. The plot looks like the following:



5. [20] Equation 4-33 in the text implies $\phi_{ms} = tpT_{PG}(E_g/2) - V_t \ln(N_A/n_i)$, where *tp* is +1(-1) for an n(p)-channel MOST and TPG = -1(+1) if a polysilicon gate is used with the same(opposite) type as the substrate. Compare this to the theoretical value $\phi_{ms} = \phi_{Gate} - \phi_{Substrate}$ (see definitions on the cover sheet). Examination of this equation reveals that it is not correct. For one thing, the substrate doping is ND (not NA) for the p-channel device. Evaluate ϕ_{ms} for the following cases (in the approximation that $E_c - E_{fi} \sim E_{fi} - E_V \sim E_g/2$) **in terms of E_g, and N_B** (which is N_D or N_A).

For n+ polysilicon, $\phi_m = \chi_{Si}$, and for p+ polysilicon, $\phi_m = \chi_{Si} + E_g$.
For the assumption that the intrinsic level is at mid-band, and for E_g in eV.
For $N_B = N_D$, $\phi_s = \chi_{Si} + E_g/2 - V_t \ln(N_B/n_i)$, and for $N_B = N_A$, $\phi_s = \chi_{Si}, + E_g/2 + V_t \ln(N_B/n_i)$

a. When $N_B = N_D$, and the gate is n+ polysilicon, $T_{PG} = -1$, $\phi_{ms} = - E_g/2 + V_t \ln(N_B/n_i)$, $tpT_{PG} = -1 \Rightarrow tp = +1$.

b. When $N_B = N_D$, and the gate is p+ polysilicon, $T_{PG} = +1$, $\phi_{ms} = + E_g/2 + V_t \ln(N_B/n_i)$, $tpT_{PG} = +1 \Rightarrow tp = +1$.

c. When $N_B = N_A$, and the gate is n+ polysilicon, $T_{PG} = +1$, $\phi_{ms} = - E_g/2 - V_t \ln(N_B/n_i)$, $tpT_{PG} = -1 \Rightarrow tp = -1$.

d. When $N_B = N_A$, and the gate is p+ polysilicon, $T_{PG} = -1$, $\phi_{ms} = + E_g/2 - V_t \ln(N_B/n_i)$, $tpT_{PG} = +1 \Rightarrow tp = -1$.

e. What change needs to be made in Equation 4-33 in order to make the *tp* parameter definition fit the first term in the ϕ_{ms} calculation?

tp = +1 for n-type substrate (p-channel devices), and *tp* = -1 for p-type substrate (n-channel devices). So the definition has to be changed to *tp* is +1(-1) for an p(n)-channel MOST

f. What change needs to be made in Equation 4-33 in order to make the sign of the $V_t \cdot \ln(N_B/n_i)$ term correct?

The term $+V_t \cdot \ln(N_B/n_i)$ in Eqn. 4-33 needs to be changed to $+tp \cdot V_t \cdot \ln(N_B/n_i)$ in Eqn. 4-33.

6. [15] A process which has $N_d = 1E15\ cm^{-3}$, $t_{Ox} = 40$ nm and $KP = 6E\text{-}5\ A/V^2$ is changed to $N_d = 1E14\ cm^{-3}$ and $t_{Ox} = 20$ nm. Estimate KP for the second process.

The change in bulk mobility is negligible in changing N_d (either the As or P doping) from 1E15 to 1E15. There will be less change in the channel mobility. The $C'_{Ox} = \varepsilon_{Ox}/t_{Ox}$ is thus the primary factor for change in $KP = \mu_o C'_{Ox}$. As a consequence,

$$KP_{40}/KP_{20} = t_{Ox,20}/t_{Ox,40} \Rightarrow KP_2 = KP_1(t_{Ox,40}/t_{Ox,20}) = 6E\text{-}5\ A/V^2(40\ nm/20\ nm) = 12E\text{-}5\ A/V^2.$$