Pentagonal Group

Standard Bipolar Process
HISTORY of SEMICONDUCTOR

- Evolved rapidly over the past 50 years
- 1\textsuperscript{st} practical analog integrated circuits appeared in 1960
- Very simple, slow, and inefficient
PROCESSSES

- Standard bipolar
- Polysilicon-gate CMOS
- Analog BICMOS
STANDARD BIPOLAR(1/2)

• 1st analog integrated circuit process
• Produced many classic devices over the years
  – 741 op-amp
  – 555 timer
  – 431 voltage reference
STANDARD BIPOLAR(2/2)

- Seldom used for new designs
- Knowledge from standard bipolar will never become obsolete
- Same devices, parasitic mechanisms, design tradeoffs, layout principles
ESSENTIAL FEATURES (1/2)

- Shaped to optimize the NPN at the expense of the PNP transistors
- NPN will outperform PNP by more than 2:1
- Early processes optimized NPN and avoided PNP transistors altogether
ESSENTIAL FEATURES (2/2)

- Employs junction isolation (JI)
JI DRAWBACKS

- Reverse-biased Jls exhibit enough capacitance to slow the operation of many circuits
- High temperatures can cause significant leakage currents
- Unusual operating conditions can forward bias the Jls and inject minority carriers into the substrate
JI ADVANTAGES

• Successfully fabricate most circuits
• Considerably cheaper than any of its alternatives
Fabrication Sequence

Starting material
- Lightly doped (111)
- P-type substrate
- Parasitic PMOS transistor
- Thick-field threshold
N-Buried Layer

- NBL mask
- Ion implantation or thermal deposition
- Arsenic or Antimony
- Discontinuity
Epitaxial Growth

- 25\(\mu\)m of n-type epi
- 45° discontinuity propagation
- NBL shadow
- Lateral shift = thickness of epi
Isolation Diffusion

- *Isolation* mask
- Heavy boron deposition followed by high temp
- Oxidation occurs
Deep-N+ (sinker)

- Deep-N+ mask
- Heavy Phosphorous deposition
- NBL diffuses upwards
- Overdrive by 25%
  - Increases doping
  - Reduces vertical resistance
  - Forms thick field oxide

- Final Junction depths
- Increased tank breakdown voltage
Base Implant

- Base mask
- Light boron implant counterdopes n-epi
- Oxide grown re-used
- BOI – base over-isolation
Emitter Diffusion

- Emitter mask
- Phosphorous deposition
- Oxide film
  - Dry oxidation
  - Wet oxidation
Contact

- Contact mask
- Etched to expose bare silicon
- Contact OR (*oxide removal*)
• Metal mask
• Aluminum-copper-silicon alloy (2% Si & .5% Cu)
• 10kÅ (1.0 μm) thick
• Metal mask
Protective Overcoat (PO)

- Compressive nitride PO
- *Phosphosilicate-doped glass* (PSG)
- PO mask
- Special etch

10kÅ (1.0 μm)
Standard Bipolar Applications

Fabrication process for:
Bipolar NPN transistors
Two types of PNP transistors:
Substrate + Lateral
Diffused resistors
Capacitors
NPN Transistors (1/2)

Composed of:

- Collector, placed in the N-epi. Tank
- Emitter + Base, described earlier
- Characteristics: MOV, EBW
Characteristics (2/2)

- Maximum Operating Voltage, up to (50 – 80v)
- Effective Base Width: E & B width
- Diode formation: CB Shorted Diode
- B & C for anode, E for Cathode
- Drawbacks: Low breakdown VEBO
- Alternative: Act as a Zener diode
- NPN is the best to be designed by this process and shows a good performance
Substrate PNP Transistor

- Previous process can not be used to form isolated PNP transistor
- Requiring P-type tank
- Substrate as Collector
- Base consist of N-tank
- Emitter = Base diff!
- No Deep (N+) diff. or NBL
Lateral PNP Transistor

• Another substitute for the isolated PNP
• Collector and Emitter regions consist of Base diff. formed into an N-tank
• E & C are self-align as only 1 masking process forms both regions
Resistors (1/4)

- Based on Characteristics Sheet resistance principle: resistance measured across a square of the material connected on opposite sides ($\Omega / \square$)
- Diffusion causes non uniform doping
- 3 types of resistors:
  - Base Resistor
  - Emitter Resistor
  - Pinch Resistor
Base Resistor (2/4)

- Ranges from 150 to 250 (Ω/?)
- Consists of a strip of B diffusion isolated by an N-tank that will reverse bias the B epi. junction
Emitter Resistor (3/4)

- A strip of E diff. Isolated by B diff. enclosed within the N-tank
- B region to reverse bias E-B junc.
- E sheet resistance less than 10 (Ω/?)
Pinch Resistor (4/4)

- Combination of B & E diffusions
- Resistor’s body consists of B diff. below the E plate (Pinched Base)
- Thin and lightly doped, resistance may exceed 5000 (Ω/?)
Capacitor (1/2)

- Thick oxide layers prevent fabricating capacitors, except when fabricating the Junction Capacitor where the depletion region of a base-emitter junction exhibits a capacitance of 0.8fF/µm². The emitter plate must be biased positively with respect to the base plate to maintain a reverse bias across the emitter-base junction.
The Base diffusion overlaps the Emitter diffusion and both are placed in a common tank.
Process Extensions

• Up-down Isolation
• Double-level Metal
• Schottky diodes
• High Sheet Resistors
• Super-beta Transistors
Up-down Isolation (1/2)
Up-down Isolation (2/2)

• **Advantages**
  – Saves space over Top-down isolation
  – Up to 15-20% of die area

• **Disadvantages**
  – PBL implant dose limited
Double-level Metal

• Advantages
  – Reduces die area by 30% over single-level metal
  – Allows component standardization

• Disadvantages
  – Requires two extra masks: vias and metal-2
  – P-Buried Layer (PBL) requires additional steps
  – Costly
Schottky Diodes (1/3)

- Silicidation and refractory barrier metallization
- Requires additional masking step
Schottky Diodes (2/3)
Schottky Diodes (3/3)
High Sheet Resistors

• Compensates for base diffusion and pinch resistor
High Sheet Resistor
Super-beta Transistors

- Beta increased by narrowing base width
- Betas of 1000 to 3000
Reference

• The Art of Analog Layout, Alan Hastings