Mechanism Failures

Group Leader
Jepsy
1) Substrate Biasing
2) Minority Injection

Asim
1) Types Of Guard Rings

Sandra
1) Parasitics
2) Field Plating

Bob
1) Minority-Carrier Guard Rings

Shawn
1) Parasitic Channel
2) Charge Spreading
What is a Parasitic Channel?

- Parasitic channel is any conductor placed above the silicon surface that can be potentially induced.
Types of Parasitic Channels

- A PMOS parasitic channel can form across any lightly doped N-type region, such as an N-tank in a standard bipolar process or an N-well in a CMOS or BiCMOS process.
An NMOS parasitic channel can form across any lightly doped P-type regions, such as the P-epi of a CMOS or BiCMOS process, or the lightly doped P-type isolation of standard bipolar processes.
What is Charge Spreading?

- Charge spreading is the mechanism underlying the formation of channels.
- It requires the presence of static electric charges at the insulating interface.
- These charges consist primarily of electrons.
- Hot carrier injection also contributes to charge spreading along with integrated circuits that do not produce hot carriers.
- Charge spreading produces parasitic PMOS transistor because it involves the accumulation of negative charges.

- High temperatures causes the accumulated static charges to disperse and restores an equilibrium between mobile ions and their fixed countercharges.
Preventative Measures

- **NMOS** channel formation can be suppressed in standard bipolar by coding base over all isolation regions.
- Standard bipolar devices are susceptible to the formation of **PMOS** channels through charge spreading.
CMOS processes use channel stop implants to raise the thick-fields thresholds.
**Field plating** consists of a conductive electrode placed above a vulnerable diffusion and biased to inhibit channel formation.
Field plates also prevent modulation of carrier concentrations in the underlying silicon by acting as electrostatic shields.

They provide excellent protection against all types of electrostatic interactions, including conductivity modulation and noise coupling from overlying leads.

Field plates also have gaps in which channels can still form.
Two methods exist for blocking gaps:

One method consists of flaring, or flanging, the ends of the field plate to elongate the channel as much as possible.

The second method bridges the gaps between the field plates with short channel stops.
Parasitics

- All integrated circuits contain parasitic components not required for operation, such as reverse-biased isolation junctions, resistances, and capacitances.

- The circuit does not benefit from the presence of parasitic components, but they can sometimes adversely affect its operation.
Parasitics

- The type of parasitics that will be discussed concern the forward biasing of junctions that normally remain reverse-biased

- Latch up
Parasitic Mechanisms

- Two important parasitic mechanisms involve currents flowing through the substrate
  - Substrate debiasing
  - Minority carrier injection
Substrate Debiasing

- Becomes a problem when currents flowing through the substrate generate voltage drops of a few tenths of a volt or more.
Substrate Debiasing Example

- This is a typical example of substrate debiasing in a standard bipolar process
Effects

- The voltage required to forward-bias a PN junction depends on both current density and temperature.
This figure depicts the cross section of a standard bipolar wafer containing a single substrate current injector and a single substrate contact.

Standard bipolar uses a lightly doped substrate and a heavily doped isolation diffusion, so $R_1 \gg R_2$. 
Types of Substrates

Lightly Doped Substrates

- Substrate resistance always increases with separation. A substrate contact placed adjacent to the injector will extract some of the current before it ever reaches the substrate.

- A substrate contact to a heavily doped isolation diffusion draws current not only from the substrate immediately beneath it but also from adjoining stretches of isolation.

Heavily Doped substrates

- Placing contacts immediately adjacent to a substrate injector can help prevent localized debiasing of the highly resistive isolation, protecting adjacent tanks from injection from the isolation sidewalls.
Preventative Measures

- Injecting little current by IC circuits into substrates will reduce debiasing and limit noise and cross-talk.

- Lateral PNP & vertical NPN transistors can inject large substrate currents when they saturate.
Heavily Doped substrates

- The contacts in the scribe seal can usually extract 5 to 10 mA without undue debiasing.

- If higher substrate currents are anticipated then the total area of contacts required can be computed using the following formula.

\[ Ac = 10 \left( \frac{p \times tepc \times Is}{vd} \right) \]
Lightly Doped Substrates with Heavily Doped Isolation

- A scattering of 10-20 sub contacts across the die will when combined with the scribe seal, handle at least 5 to 10 mA.

- Sensitive low-current circuitry should reside at least 250um away from any substantial source of substrate injection, since debiasing on lightly doped substrates tends to localize around the point of injection.
Lightly Doped Substrates with Lightly Doped Isolation

- Large numbers of substrate contacts scattered across the die will help extract substrate current, but some degree of localized substrate debiasing is inevitable.

- Sensitive circuits should be located far away from major sources of substrates injection.

- Since substrate modulation can inject substantial noise into high-impedance circuitry consider placing wells under resistors and capacitors to isolate them from substrate noise coupling.
Minority Carrier-Injection

- Junction isolation relies on reverse-biased junctions to block unwanted current flow.

- The electric fields set up by depletion regions repel majority carrier, but they block the flow of minority carrier.

- Many of these recombine, but some eventually find their way to the depletion regions isolating other devices.
- The tank pulled below ground acts as the emitter of lateral NPN transistor Qp.

- Substrate contacts cannot, by themselves, stop minority carrier injection since minority carriers travel by diffusion and not by drift.
Substrate Injection
Preventive Measures (Substrate Injection)

- Eliminate the forward-biased junctions
- Increase the spacing between components
- Increase doping concentrations
- Provide alternate collectors to remove unwanted minority carriers
Electron-collecting minority-carrier guard ring.
Cross section of two electron collecting guard rings.
Cross section of an improved minority-carrier guard ring for collecting electrons.
Cross section of a minority-carrier guard ring for collecting holes injected into the tank.
(Hole collecting guard ring)
What is a hole collecting guard ring?

- It is a first line of defense against hole injection into the substrate, the tank is floored with NBL and ringed with deep N+.
- It is a base ring placed just inside the deep N+. This ring usually connects to ground, but it will remain reasonably effective even if it is tied to the tank terminal.

- Any hole impinging on the depletion region surrounding the base region will be drawn across by the electric field. Holes become majority carriers inside the base diffusion and can be removed through contact.

- This ring collects up to 90% of the holes and is largely ineffectual without NBL.
Cross-Injection (circuit failure)

- **What is it?**
- It is the injection of minority carriers in its own tank or well. (like PMOS transistor, HSR resistor or a lateral PNP collector).
- This problem can be avoided by placing each transistor in its own tank or well, but this wastes a lot of area resulted in the end with isolation diffusion.
- Therefore a P-bar or N-bar (another minority carrier guard ring) are more suitable for such fields.
What is a P-bar?

- It’s a minimum width strip of base diffusion placed between two transistors (PNPs).

★ A wider P-bar can increase collection efficiency by diffusing deeper into the epi.
Other Applications of P-bars:

- In Bipolar (in lateral PNP transistors.)
- CMOS processes use P-moat (type of P-bar)
- NPNs driving either a lateral or a substrate PNP transistor, in which the collector of the NPN connects to the base of the PNP. (suppresses latch up)
What is an N-bar?
- It consists of a strip placed between two devices occupying a tank.
Problems:

- N-bar has very less P-isolation on either side, therefore it can lead to break down at low voltage.
- Also the gaps allow minority carriers to by pass the N-bar, therefore it exhibits lower collection efficiency.