Capacitors in IC design

- Coupling AC Signals
- Constructing timing networks
- Constructing phase shift networks
- Feedback loop compensation
- Semiconductors use:

\[ 10^{-12} \leq C \leq 10^{-6} \]
Parallel Plate Capacitor

\[ C = 0.0885 \cdot \frac{(A \cdot \varepsilon_r)}{t} \]

\( \varepsilon_r \) – dielectric constant

A – Area of electrode \([\mu m^2]\)

\( t \) – thickness of the dielectric \([\text{Angstroms}]\)

• If plate area A is 0.1mm\(^2\) with 200 Å dry oxide film and \( \varepsilon_r \) is about 4,
  • Then C will be about 180 pF
Maximizing Capacitance

• Decreasing thickness $t$ will cause $C$ and $E$ to go up, this can:
  - Break covalent bonds
  - Cause avalanche multiplication in resulting carriers
  - Leads to damage in dielectric molecular Structure
  - Eventually shorts the capacitor

• So, $E < \text{dielectric strength}$

$$V_{max} = 0.01 \cdot t \cdot E_{crit}$$

• A 200 Å dry oxide can withstand approx. 20V derated by %50
Maximizing Capacitance contd.

• High permittivity dielectrics
  – Barium strontium titanate and other ceramics have $\varepsilon_r >> 1000$
  – Silicon nitride $\varepsilon_{r, \text{silicon nitride}} \sim 2^{*}\varepsilon_{r, \text{oxide}}$

• Composite dielectrics
  – Sandwich nitride between two oxides for less pinholes

$$\varepsilon^\text{eff} = \frac{(t_{ox} + t_{nit})}{\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \left(\frac{t_{nit}}{\varepsilon_{nit}}\right)}$$

  – If 200 Å of nitride and $\varepsilon_r = 7.5$ is sandwiched between two 50 Å oxide films with $\varepsilon_r = 3.9$, $\varepsilon^\text{eff} = 5.7$
Oxide/oxide-nitride dielectric Capacitors

• Thin film capacitors
  – Oxide Capacitor
  – ONO Capacitor
  – Poly-poly Capacitors
  – MOS capacitor
    • Gate oxide capacitor
Capacitance Computations

• Maximum capacitance in thin film capacitors depends only on the dielectric in use.

• With overlapping electrodes, common area is used in the following equation to determine C.

\[ C = 0.0885 \cdot \frac{(A \cdot \varepsilon_r)}{t} \]
Junction Capacitors

• Use the depletion region as a dielectric
  – Higher permittivity
  – Extreme voltage non-linearity due to depletion region
    variation in width with applied bias.

• $C_{j0}$ (zero-bias capacitance) serves as a measure
  of the capacitor, which can be computed using:

\[
C = 0.0885 \cdot \frac{A \cdot \varepsilon_r}{t}
\]

• In the case of an abrupt junction between a
  heavily doped region and a lightly dope region:

\[
W_o \sim 3.10^{11} \sqrt{1/N} \text{ [Å]}
\]

$W_o$ - Depletion region width
Junction Capacitors \textit{contd.}

- Area of junction capacitor

- $X_j$ is the junction depth
- $A_d$ - Area of oxide window
- $P_d$ - perimeter oxide window

$$A_{total} = A_d + \left(\frac{\pi}{2}\right) \cdot x_j \cdot P_d$$
Junction Capacitors *contd.*

- $A_d$ - Area of oxide window
- $P_d$ - perimeter oxide window
- $C_a$ - Capacitance per unit area
- $C_p$ - capacitance per unit periphery

\[
C_{\text{total}} = C_a \cdot A_d + C_p \cdot P_d
\]
Junction Capacitors *cont'd.*

- Two types primarily used are comb (B) and plate (A) capacitors
Conclusion

• In practice, comb capacitors appear more on older analog circuit layouts.

• They rarely appear on CMOS and BiCMOS design due to thin film capacitors, which can provide equal capacitance with less parasitics associated.
CAPACITOR VARABILITY
What is the cause of Capacitor Variation?

Mostly:
- Process Variation
- Voltage Modulation

Also:
- Electrostatic Fields
- Fringing Effects
- Doping and Thickness
Dielectric consists of a thin film of silicon dioxide grown on monocrystalline silicon.

- Film ranges from 100A-500A
- ±20% on average
- ±10% best case
Dielectrics are formed by a three-step process consisting of initial oxide growth followed by nitride deposition and subsequent surface oxidization.

±20% on average
Process Variation
Junction Capacitor

- Constructed from base and emitter diffusions
- Junction depth and doping factors effects depletion region width
- ±20% variation on average
Voltage Modulation

• Ideally, the value of a capacitor would not depend on the bias placed across it

• MOS and Junction capacitance is affected by the voltage

How does voltage effect capacitance?
Voltage Modulation MOS

- The capacitance varies only slightly as the MOS capacitor goes into reverse-bias.
- The capacitance goes less than 20% and holds as a forward-bias voltage is applied.
- The capacitance will restore at higher bias if source and drain are connected to the backgate.
Voltage Modulation
MOS

Capacitance

Capacitance is constant in accumulation

Capacitance recover at higher bias if source and drain are connected to the backgate

Capacitance remains low if source and drain are unconnected

Capacitance reaches a minimum at the threshold voltage
Voltage Modulation
Junction Capacitor

• Capacitance gradually decreases from Cjo as the reverse-bias increases
• Junction avalanches at -7V
• Capacitance increases as the voltage approaches .7V to its maximum
• Beyond .7V the capacitance falls sharply
Voltage Modulation
Junction Capacitor

Capacitance peaks at about 0.7V
Capacitance becomes difficult to measure due to forward conduction

Junction avalanches at about -7V

Reverse-bias 0 Forward-bias
Conclusion

• Junction and MOS capacitors have one electrode formed of lightly doped silicon that is prone to depletion modulation, thus voltage variation results

• Other capacitors, using highly conductive electrodes exhibit a small voltage modulation
CAPACITOR PARASITICS
Capacitance Parasitics of Transistors
Capacitor - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

Top Plate parasitic is 0.01 to 0.001 of $C_{\text{desired}}$

Bottom Plate parasitic is 0.05 to 0.2 $C_{\text{desired}}$
Subcircuit Models

- Junction Capacitor
- MOS or Gate Oxide Capacitor
Vertical MOS Transistors

- The channel length is not defined by lithography
- Are easily made with both front gate and back gate
- The possibility to prevent short channel effects
Surface Mount Technology

• Can reduce inductance by half
• Example for 0.1uF. L goes from 1000pH to 500pH
CAPACITOR COMPARISON
Base-emitter Junction Capacitors

- Capacitance of 0.5pF/mil to 0.8pF/mil
- Capacitance falls off with reverse bias
- Effective capacitance of 0.3pF/mil
Base-emitter Junction Capacitors

- Disadvantages
- Extreme variability of capacitance values
- Low breakdown voltage (6.8V)
- Forward bias for increased capacitance
MOS Capacitors
MOS Capacitors

- Uses MOS transistor as a capacitor
- Normally biased at 1 volt to remain in the linear region of the capacitance curve
MOS Capacitors

- Disadvantages
- MOS transistors are not well suited for use as capacitors
- Substantial series resistance
- Electrodes are not interchangeable
Poly-poly Capacitors
Poly-poly Capacitors

- Uses polysilicon for both plates separated by oxide
- Using a nitride layer results in higher capacitance values
- Large plate area oxide capacitor useful for matching capacitors
- Low voltage modulation
Poly-poly Capacitors

- Disadvantages
- ONO composite dielectrics experience hysteresis effect above 10MHz
- Plates are not interchangeable
Miscellaneous Capacitors

- Thin film using metal for upper plate
- Silicided lower plate with metal upper plate
- High permittivity materials
  - Tantalum pentoxide
  - Ceramic thin-film dielectrics