Chapter 7.2.7.-7.3.2.

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Temperature Gradients and Thermoelectrics

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All semiconductor devices have temperature coefficients.

But, what are they and how are they measured.

well, lets take a look........
An example to consider…..

- 1kΩ resistor, 10mA through it will dissipate 100mW
- Thermal Z = 80°C/W
- Temp Coefficient = 3000ppm/°C = (3*°C)/1000
- The result is an 8°C rise and a 2.4% increase in resistance
Electrical Properties and Temperature

- The concept:
  - Temperature variations cause variations in the resistance of the resistor

- Consider the following:
  - $T_j = T_a + P_d \cdot ja$
  - $T_j = T_c + P_d \cdot jc$

- $T_j =$ junction temp, $T_a =$ ambient temp, $T_c =$ case temp, $P_d =$ power dissipation, $ja =$ junction-to-ambient thermal impedance
So knowing this……
Which is best for semiconductor applications?

The lower thermal impedances?
- Dissipates heat slowly
- Virtually equal heat dissipation

The higher thermal impedances?
- Dissipates heat rapidly
- Very Unequal heat dissipation
And the answer is......

The lower thermal impedances

• True, lower thermal impedances equals an increased overall temperature.
• But this is accepted because of the equally distributed temperature.
• Not perfect, but you take what you can get.
Isothermal contour plot
Thermal Gradients

- Depend on isothermal spacing
- (Thermal mismatch between two devices) = (the linear temperature coefficient) * (the distance between the centroids of the resistors) * (the thermal gradient along a line connecting the centroids of the resistors)
Arrangement of power devices

(A) Acceptable

(B) Optimal

(C) Optimal

(D) Optimal
Resistor Connections

(A)

(B)
Resistor Contact Placement

(A)

(B)

(C)
Electrostatic Interactions

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Electrostatic Interactions

• Electrostatic fields reduce value of both capacitors and resistors.
  – E-fields cause accumulation depletion of carriers in a resistive material.
  – Coupling of capacitors to surrounding circuitry via fringing fields can cause unexpected values in capacitance.

• Electrostatic interactions in Resistors:
  – Voltage modulation
  – Charge spreading
  – Dielectric polarization

• Electrostatic interactions in capacitors:
  – Fringing fields
  – Dielectric relaxation
Voltage Modulation

- R values are affected by voltage present on adjacent nodes of the circuit.

- Tank Modulation
  - Value of diffused R’s may vary with voltage differential between the tank and resistor body.
    - As $V_{\text{TANK-RESISTOR}}$?, depletion region widens, and R increases.
  - Matched resistors may reside in a common tank only if they have equal R values and experience the same bias.
  - Different valued resistors must be placed in their own individually biased tank.
  - Mismatch can be minimized by using low sheet diffusions such as base or emitter rather than HSR.
    - Matched base Resistors can be put in common tanks.
Voltage Modulation

• Leads routed over resistors can also effect operation.
  – These leads couple noise into the resistor.
  – E-field between leads and resistors may cause **conductivity modulation**.
  – HSR experience more conductivity modulation, impact of conductivity modulation depends on:
    • Voltage between a lead and an underlying resistor
    • The thickness of the intervening oxide.
    • The area of intersection
  – Leads should not be routed over critically matched resistors
Showing placement of a jumper between resistor segments in a single-level metal process
Voltage Modulation

• Leads may cross resistors if electrostatic shielding is used.
  – This prevents conductivity modulation.
  – Also prevents capacitive coupling
  – Allows a more compact layout
Electrostatic Shielding
Electrostatic Shielding

- Leads can cross the shielded resistors without modulating the conductivity.
- All leads should reside away from the edges of the shield.
- The shield also helps minimize stresses generated in the poly resistors by the presence of second metal leads running across them.
Electrostatic Shielding

- A common shield will do as long as voltage difference across the array remains small and sheet resistance < 500Ω.

- The shield could be divided up into individual sections to be placed over each resistor.
  - Each shield must overlap its respective resistor by several microns to ensure fringing fields do not degrade its effectiveness.
  - Sectioned shielding requires more space than common shielding.
Electrostatic Shielding

- The substrate can also inject noise coupling into deposited resistors and capacitors.
  - A well may be placed underneath the components and connected to AC ground
  - The well does not do much good in most cases because only the 1st few microns of the substrate are penetrated. The substrate can be hundreds of microns deep.
Charge Spreading

- Circuit operation injects electrons into oxide overlying the die.

- Some of these electrons become trapped in the interface between the interlevel oxide and the protective overcoat.
  - They may also become trapped between the overcoat and the mold compound
  - These mobile electrons may vary resistor values through conductivity modulation.

- Matched High Sheet Resistors are extremely susceptible long-term drifts caused by charge spreading

- Base resistors are much less susceptible to charge spreading to their low resistance.
Minimizing Charge Spreading

- Electrostatic shielding can eliminate the effects of charge spreading on matching.
- Some of these electrons become trapped in the interface between the interlevel oxide and the protective overcoat.
  - They may also become trapped between the overcoat and the mold compound

- These mobile electrons may vary resistor values through conductivity modulation.
- Matched High Sheet Resistor are extremely susceptible long-term drifts caused by charge spreading
Minimizing Charge Spreading

- Electrostatic shielding serves as a field plate counteracting surface inversion across high-voltage tanks
- **Field plating** consists of a conductive electrode placed above a vulnerable diffusion and biased to inhibit channel formation.
  - Noisy signals must not be routed across field plates unless the field plates connect to low impedance nodes which are insensitive to capacitive coupling
Minimizing Charge Spreading

- Field plates prevent channel formation by flanging over the body of the resistors.
- Area required for diffused HSR resistors make them uneconomical compared to deposited resistors.
Dielectric Polarization

- **Dielectric polarization** rises due to the movement of charges within an insulator.

- Mobile ions slowly redistribute under the influence of an external E-field.

- E-field at the surface of the Si shifts over time as ions assume a new configuration.

- When the external E-field vanishes, the new distribution of mobile ions creates an E-field in the opposite direction to the original.

- This slow variation in the E-field is extremely undesirable and can modulate the value of a high-sheet resistor.
Preventing Dielectric Polarization

- **Field Plating** is usually not a good option due to the deliberate E-field induced across the interlevel oxide.

- Leaving the plates off renders resistors vulnerable to charge spreading.

- If using HSR is absolutely necessary, then the alternative using split field plates.
Preventing Dielectric Polarization

- Gap between plates falls on the center of each resistor
- The split field plate subjects the half of the resistor to an e-field equal and opposite to that on the other end, so cancellation of e-field occurs.
- Split field plates are recommended if resistors have sheet resistances of exceeding 1 kΩ and must match to better than ±0.5%
Dielectric Relaxation and Charge Spreading in Capacitors

- Dielectric relaxation is much like dielectric polarization in resistors.
  - Timing circuits and sample hold circuits are intolerant to this.

- Charge spreading affects capacitors much like it affects resistors.
  - Capacitor being charged causes a shifting E-field, which in turn cause gradual redistribution of charges along insulating interfaces.
Dielectric Relaxation and Charge Spreading in Capacitors

Cross section of a poly-poly capacitor incorporating an electrostatic shield plate
Rules for Resistor Matching

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Resistor Matching Rules

- Construct matched resistors from a single material
- Make matched resistors the same width
- Make matched resistors sufficiently wide
- Where practical, use identical geometries for resistors
- Orient matched resistor in the same direction
Resistor Matching Rules

• Placed matched resistors in close proximity
• Interdigitate arrayed resistors
• Place dummies on either end of a resistor array
• Avoid short resistor segments
• Connect matched resistors in order to cancel thermoelectrics
Resistor Matching Rules

- If possible, place matched resistors in low stress areas
- Place matched resistors well away from power devices
- Place precisely matched resistors on axes of symmetry of the die
- Consider tank modulation effects
Resistor Matching Rules

• Sectioned resistors are superior to serpentines
• Use poly resistors in preference to diffused ones
• Place deposited resistors over field oxide
• Choose P-type poly resistors in preference to N-type poly resistors
Resistor Matching Rules

• Do not allow the N-buried layer (NBL) shadow to intersect matched diffused resistors
• Consider field plating and electrostatic shielding
• Avoid routing unconnected leads over matched resistors
Resistor Matching Rules

• If leads cross resistors, they should cross all resistor segments in the same manner
• Avoid excessive power dissipation in matched resistors.
Rules for Capacitor Matching

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Capacitor Matching Rules

1. Use identical geometries
   - Different sizes of capacitors match poorly
2. Use square geometries for precisely matched capacitors
   - Peripheral variations are major source of random mismatch
   - Lowest periphery to area ratio
Capacitor Matching Rules

3. Make capacitors as large as possible
   - Optimum size between 20 x 20 to 50 x 50 um

4. Place matched capacitors adjacent to one another
   - Large number of capacitors should be placed into rectangular arrays
Capacitor Matching Rules

5. Place matched capacitors over field oxide
   - Surface discontinuities will cause variations in capacitor topography

6. Connect upper electrode to higher impedance node
   - Upper electrode normally exhibits less parasitic capacitance
Capacitor Matching Rules

7. Place dummy capacitors around outer edge of array
   - Dummy capacitors will shield matched capacitors from lateral electrostatic fields and eliminate variations in etch rates
Capacitor Matching Rules

8. Electrostatic shield matched capacitors
   - Contains fringing fields
   - Allows leads to go over capacitors
   - Shields capacitors for electrostatic fields
   - Reduces effects of packaging stress
Capacitor Matching Rules

9. Cross couple arrayed capacitors
   - Minimizes the effects of oxide gradients

10. Consider capacitance of leads
    - Leads will contribute to capacitance

11. Avoid running leads over unshielded capacitors
Capacitor Matching Rules

12. Use thick oxide dielectrics
   - Thick oxides exhibit less dimensional variation

13. Place capacitors in areas of low stress
   - Place capacitors in area from center of die to halfway out
Capacitor Matching Rules

14. Place capacitors away from power devices
   - Should be 200 to 300 um from power devices

15. Place capacitors on axes of symmetry
   - On (100), arrays should align with axes of symmetry on die. On (111), arrays should lie on <211> axis