I. The Standard Bipolar NPN Transistor

1. Heavily doped emitter; a precisely tailored base profile; a thick, lightly doped N-epi; a heavily doped NBL; and a deep-N+ sinker. Figure 8.13 show the key features of NPN transistor

![Figure 8.13 Key features of the standard bipolar vertical NPN transistor.](image)

1) Heavily Doped Emitter
   i. Doped with phosphorus to max. Efficiency
   ii. Arsenic is used to compensate for lattice strains induced by the heavily doped phosphorus doping
   iii. Arsenic factor eliminates defects that might migrate into neutral base and degrade the beta of the transistor

2) Bipolar Base Diffusion
   i. Provide High Beta, high Early Voltage, and moderate $V_{CEO}$
   ii. Lightly doped base also increases the planar $V_{CEO}$ and $V_{CEO}$ of the vertical NPN
   iii. Must contain sufficient dopant to allow Ohmic contact since no shallow P+ diffusions exist in the process
   iv. Too low a doping concentration can cause surface inversion and parasitic channel formation that can reduce the low current beta of the transistor

3) N-epi, N+ Buried Layer, Deep-N+ sinker
   i. Lightly doped layer increases $V_{CEO}$ and and Early voltage by allowing formation of a wide depletion region extending into collector
   ii. his drift region lies sandwiched between the base and a heavily doped extrinsic collector
   iii. Drift region consists of remaining lightly doped N-epi beneath the base and above the NBL
   iv. Extrinsic collector consists of NBL and the deep N+ sinker
v. D.R. depletes through at higher currents due to velocity saturation and at higher collector to emitter voltages due to extension of base collector depletion region

vi. Quasisaturation- effective resistance of the neutral collector increases due to a range of collector voltages and currents that cannot deplete the D.R.

vii. Can be minimized by keeping DR as this as possible consistent with $V_{ceo}$ rating

viii. NBL creates low resistance path across the bottom of the transistor, but current still flows upward

ix. Lightly doped epi separating contact from NBL is highly resistive, so the inclusion of a deep N+ sinker can reduce the total collector resistance

x. Power transistors always include deep-N+, small signal devices often omit it

II. Construction of small signal NPN transistor

1) Square or rectangular emitters

2) There are two styles of NPN transistor structures
   a) Collector-emitter-base (CEB) shown as below
   b) The function of CBE slightly reduces the collector resistance
   c) The CEB will outperform the CBE
d) Collector-base-emitter (CBE) shown as below

3) The typical structure of the device uses in circuit with a 5Ω-cm, 17μ layer
   a) The emitter diffusion is 20μ×25μ
   b) The base diffusion is 45μ×60μ
   c) The base-isolation spacing is 20μ
4) Scaling factors that are less important are lateral conduction, current crowding, and emitter push
5) Transistors with large area to periphery ratios usually have higher betas than those with smaller
   a) The smaller transistor exhibited a peak beta of 290
   b) The larger transistor exhibited a peak beta of 520
6) Large emitters drive deeper into the base diffusion, thus reducing the neutral base width
7) Emitter contact occupies as much of the emitter area to minimize emitter resistance
8) Emitter diffusion should overlap contact equally on all sides to ensure uniform lateral current flow
9) Base diffusion must overlap the emitter on all sides to prevent lateral punchthrough
10) The outdiffusion of the P+ isolation determines the minimum tank overlap of base diffusion
11) Base region occupies a tank contacted at one end by a deep-N+ sinker
12) Regardless of whether a sinker is used, the NBL should fill as much of the tank as possible to minimize the overall collector resistance
13) If transistor must conduct more than a few milliamps, the transistor should be enlarged to allow the NBL to completely enclose the deep-N+ sinker.

14) Many variations exist for NPN layout, epi for single level metal processes.

15) Lack of second metal forces designer to route leads through the transistor.

16) Transistors can be stretched to allow one or more leads to route between their terminals.

17) Stretched transistors exhibit increased base and collector resistances and capacitances that could interfere with proper circuit operation, so stretching is avoided.

18) Three typical stretched-transistors:
   a) Figure A shows stretched-collector-transistor
      i. Collector and base contacts have been moved apart to allow two leads to pass between them.
      ii. This will increase the collector-resistance and collector-substrate-capacitance.
   b) Figure B and C shows stretched-base-transistor
      i. The base region has been elongated to allow two leads to pass between.
      ii. This will increase the base-resistance and collector-base-capacitance.

19) Double level metal (DLM) eliminates the need for stretched transistors.

20) It eliminates stretched devices and tunnels, and also it reduces the die area.

21) DLM also allows the use of a small number of standardized layouts that can be fully characterized and modeled to enable more accurate simulation.

22) Many ways for Scaling up NPN transistors in order to increase emitter area without reducing performance.

23) Long narrow, emitter stripes or fingers.

24) Base contacts placed along both sides of each emitter finger help minimize base resistance, increasing switching speed and enhancing immunity to secondary breakdown.
25) Relatively small area to periphery ratio yields a lower beta than that of a compact emitter NPN
26) This narrow emitter becomes vulnerable to thermal runaway at emitter current densities
27) Narrow emitter provides superior frequency response, but inferior beta to compact
28) Narrow is not suitable for power devices

III. The Standard Bipolar Substrate PNP Transistor

1) NPN and PNP transistors differ only in doping polarities, so a PNP transistor can be created by inverting all of the doping polarities of the standard bipolar process
2) The collector consist of lightly doped P-type epi with the addition of a P-buried layer(PBL) and a deep-P+ sinker
3) Base- lightly doped N-type diffusion and the emitter of a heavily doped P-type
4) Standard bipolar NPN transistors employ heavily doped emitter to maximize efficiency
5) Standard Bipolar cannot fabricate a fully isolated vertical PNP transistor
6) Standard bipolar offers a type of vertical PNP transistor called substrate PNP
7) Substrate PNP lacks full isolation because it employs the P-type substrate as its collector
8) Base consists of N-epi and its emitter of base diffusion

9) The performance suffers because materials are not tailored to their respective tasks
10) Substrate PNP requires no steps, and costs nothing to add one to a standard bipolar design
11) The emitter of a substrate PNP consists of base diffusion and the base consists of a n N-tank contacted by means of emitter diffusion
12) In the absence of NBL, the epi-substrate junction diffuses upward during the long isolation drive
13) The base region of the substrate PNP is both thin and lightly doped
14) Minimum-emitter substrate PNP typically exhibits 100Ω of emitter resistance
15) The peak beta are 100 or more
16) High-level injection cause their betas to peak at current densities of less than 1mA/mil^2
17) The collector consists of a series combination of P-substrate and p+ isolation diffusion
18) The collector current does not exceed 1 or 2mA
19) The total collector current does not exceed 10mA
20) Substrate PNP transistors become more impractical as current levels increase
21) Lateral PNP transistors can be substituted for high-current substrate devices to minimize substrate debiasing
22) Substrate PNP transistors operate primarily by vertical conduction
23) Precise scaling depends on outdiffusion, lateral conduction, and surface effects
24) As with vertical NPN transistors, precisely matched substrate PNP transistors must identical emitter geometries

IV. Construction of Small-signal Substrate PNP Transistors
1) Three styles of substrate PNP transistor shown as figure 8.19
   a) Figure 8.19A
      i. The collector current does not exceed a milliamp or two
      ii. Higher corrector will probable debias
   b) Figure 8.19B
      i. The emitter-ringed transistor exhibits a higher beta at low current
      ii. The base forward-biases into the emitter ring at high current densities
   c) Figure 8.19C
      i. Sometimes called a tombstone PNP or cathedral PNP
      ii. The base ring helps counteract the high sheet resistance of the periphery of the isolation
      iii. Requires much the field plating

FIGURE 8.19 Examples of (A) standard, (B) emitter-ringed, and (C) vertical styles of substrate PNP transistor.
2) The tank serves as base and base diffusion as emitter
3) Emitter diffusion beneath base terminal allows Ohmic contact to tank
4) Larger and more compact emitter structures produce higher gains
5) Figure 8.20 is the layout of a larger substrate PNP transistor

![Figure 8.20](image)

**V. The Standard Bipolar Lateral PNP Transistor**

1) Although standard bipolar cannot fabricate an isolated vertical PNP, it does offer an isolated lateral PNP consisting of 2 separate base diffusions placed in a common tank

   a) One of these diffusions serves as the emitter and the other as the collector
   b) Lateral transistors have slower switching speeds and lower beta than vertical devices
   c) A narrower basewidth produces a higher beta and a lower Early voltage, while a wider basewidth produces the opposite effect
   d) The product of beta and Early voltage remains approx. constant regardless of bandwidth

2) The beta of lateral PNP depends on emitter injection efficiency, base doping, base recombination rate, base width, and collector efficiency

   a) Only base width and collector efficiency can be controlled by designer
   b) The emitter injection efficiency suffers from the use of the relatively lightly doped base diffusion as the emitter
3) The standard bipolar lateral PNP transistor suffers from elevated recombination rates caused by the use of (111) silicon

   a) Annealing in a reducing atmosphere, such as foaming gas, reduces the surface state concentration and increases the beat of the lateral PNP transistor at the cost of reducing the thick field threshold
   b) Together with smaller feature sizes, reducing anneals increased the peak beta of standard bipolar lateral PNP transistors from less than 10 to more than 50

4) The drawn basewidth of a lateral PNP equals the separation between the drawn base diffusions serving as its emitter and collector, \( W_{B1} \)

   a) The actual base width of the transistor is difficult to determine because it depends on two dimensional current flow
   b) Near the surface, the actual base width \( W_{B2} \) is considerably less than the drawn base width \( W_{B1} \) due to outdiffusion
   c) The effective base width of the transistor consists of a weighted average of all possible paths by which carriers might traverse the neutral base
   d) The effective base width consists of the drawn base width minus twice the outdiffusion distance, or \( W_{BJ} \)
   e) The effective base width substantially exceeds the actual base width at the surface due to the contribution of subsurface conduction
   f) The Early voltage of a lateral PNP is inversely proportional to peak beta

5) The gain of a lateral PNP appears to increase when NBL is placed underneath the emitter

   a) Increase occurs because NBL restricts the motion of holes to a smaller region of the N-epi and reduces recombination
   b) NBL also greatly increases collection efficiency by blocking the injection of holes into the substrate
6) Some percentage of the emitted carriers does not escape by traveling laterally beneath the collector diffusion while the transmitter remains in the normal active region

   a) The NBL updiffuses through the epi, establishing a retrograde doping profile that tends to drive the minority carriers upward along the built-in potential gradient

   b) The depletion region surrounding the collector reaches deep into the lightly doped N-epi and intercepts a large fraction of minority carriers attempting to pass underneath it

   c) Only a small percentage of emitted carriers successfully escape the collector to reach the isolation sidewall

   d) Transistors with shallow collector regions may experience greater sidewall losses

VI. Construction of Small-signal Lateral PNP Transistors

1) The lateral PNP transistor consists of a small plug of base diffusion surrounded by a larger annular base region

   a) The central base plus serves as the emitter of the transistor, while the surrounding base ring serves as its collector

   ![Figure 8.22](image)

   **Figure 8.22** Layout of a lateral PNP transistor showing emitter field plate.
b) In reverse mode, the outer ring of base becomes the emitter and the majority of the injected carriers are injected toward the isolation sidewalls rather than to the small base plug in the center of the transistor
c) Despite identical doping levels in emitter and collector, the lateral PNP transistor remains a profoundly asymmetrical device

VII. Summary of Device Characteristics

1) Electrical characteristics of the lateral PNP transistor depend on the particular fabrication process used
2) With reference to the three basic bipolar processes (low-, medium-, and high-voltage processes), the two key parameters which affect the lateral PNP transistor are the epitaxal resistivity and the collector-emitter spacing (base width)
3) Use of lightly doped n-type epitaxal region of the NPN transistor as the base region
4) Inferior to the basic NPN transistor in their current handling or high frequency characteristics
5) Extremely useful in biasing, dc level shifting and serving as active load devices in gain stages
6) The base region of the device is formed by the n-type epitaxal layer which serves as the collector of the NPN transistors
7) The p-type base diffusion of the NPN transistor is used to form the emitter and collector regions of the lateral PNP transistors
8) The n⁺-type emitter diffusion transistor is used to form the n⁺-type contact region for the PNP base
VIII. High Voltage Bipolar Transistors

1) The maximum operating voltage of a process cannot exceed that of its weakest device

   a) In standard bipolar processes, the vertical NPN transistor usually breaks down before the either the lateral of the substrate PNP
   b) The NPN Vceo determines the maximum operating voltage
   c)
\[ V_{CEO} = \frac{V_{CBOP}}{\sqrt{\beta_{max}}} \]

   Where:
   i) \( V_{CBOP} \) is the avalanche voltage of the planar base collector junction
   ii) \( \beta_{max} \) represents the peak beta of the device
   iii) \( n \) is the avalanche multiplication factor which usually lies in the range \( 3 < n < 6 \)

   d) Epi thicknesses are usually offered corresponding to convenient operating voltages, such as 20V, 40V, and 60V
   e) If a process offers a choice of voltage ratings, use the lowest one possible because the higher voltages require larger isolation spacing

2) Parasitic channel formation and charge spreading become increasingly serious concerns at higher voltages

   a) At voltages exceeding the thick-field threshold, metallization can directly induce parasitic channel formation and complete field plates and channel stops become mandatory for proper circuit operation
   b) The exposed surface of the base region between the emitter and the collector of a lateral PNP transistor should always be field-plated regardless of operating voltage

3) The breakdown voltage of any junction depends on its curvature, the sharper the curvature, the lower the breakdown voltage

   a) Deeper junctions exhibit higher breakdown voltages
   b) The observed breakdown voltages of shallow junctions often depend on geometry because the curvature of the corners of the diffusion exceeds the curvature of the sidewalls
   c) Because designers must push the operating voltage of base or HSR diffusion close to its limits, he must round off the corners with a small arc, or fillet, to achieve full operating voltage
   d) Fillets, however, sometimes produce false diagnostics during verification, so some designers use chamfers
   e) Chamfer – small diagonal facet drawn perpendicular to a line bisecting the vertex
4) Higher voltage layouts often require increased spacings between certain diffusions to accommodate wider depletion region widths

   a) Spacings that require modification include base-base, HSR-HSR, base-HSR, base-iso, and HSR-iso
   b) One should use a higher voltage process rather than attempting to push the ratings of a lower voltage one
TERMS TO KNOW

Avalanche Breakdown – the field in the collector-base depletion region becomes strong enough so that the free electrons break covalent bonds when they collide with the crystal lattice.

Beta – For BJT amplifier:

\[ \beta = \frac{i_c}{i_b} \]

We desire base current to be small compared to the collector current, so we want a high value for \( \beta \).

Carriers – holes and electrons transporting electric charge, move under the influence of electric fields.

Diffusion – motion of carriers through a silicon crystal that occurs at all times and places.

DLM – (Double level metal) virtually eliminates the need for stretched transistors and tunnels, also reduces the die area because metal jumpers and vias can reside on top of other devices.

Doping – addition of certain impurities to semiconductors to greatly increase the number of available carriers, can approach the conductivity of a metal.

Depletion Region – After a junction is formed, holes diffuse from the p-side to the n-side, and the electrons diffuse in the opposite direction. This causes negative charge to build up on the p-side of the junction, and vise versa for the n-side. This electric field created is the depletion region.

Early Voltage – when examining the common-emitter characteristics with exaggerated secondary effects, the straight-line extensions all meet at a point on the negative Vce axis, the voltage magnitude at this intersection is called the Early Voltage.

HSR – (High Sheet Resistor) a shallow, lightly doped p-type implant, provides low current circuits with more resistance than the base diffusion can and more precision than the pinch resistors can achieve.

NBL – (N-type Buried Layer)

Ohmic Contact – contacts made between metals and semiconductors in order to connect solid-state devices into a circuit, they exhibit a small amount of resistance.
Parasitic Channel—when a conductor bridges two diffusions, then a leakage current can flow through the channel from one diffusion to the other, most parasitic channels are relatively long and cannot conduct much current

PBL – *(P Buried Layer)*

Quasisaturation – *an effect when collector voltages and currents cannot entirely deplete the drift region, causing the effective resistance of the neutral collector to increase*

Sinker – *(deep-N+) allows low-resistance connection to the NBL*