Instructor: Professor Ronald L. Carter, ronc@uta.edu, http://www.uta.edu/ronc, 532 Nedderman Hall, (office hours: Tu/W 11 AM to noon), 817/272-3466, fax 817/272-2253.

Course Learning Goals and Objectives: Design principles for electronic circuits and systems based on semiconductor integrated circuits. Will include cell and circuit development using CAD/CAE design tools. Both physical and behavioral model design will be utilized. Integration of semiconductor electronics principles, process principles and design, and simulation in the open-ended design of microelectronic circuits and systems. The class will be conducted using a project/entrepreneurial model to simulate the environment of the real world engineering business environment.

Class Meetings: Tu/Th, 1230-150pm, 108 Nedderman Hall

Teaching Assistant: Ms. Sonali Kulkarni, sonkul@hotmail.com, 254 NH, Tu/Th 2:30 to 4 PM, 817/272-2351.

Attendance Policy: Attendance at every class session for the entire 80-minute period is strongly advised.


Analog Design Reference Texts: (Books on reserve in the Science and Engineering Library are marked R.)

Spice References: (Books on reserve in the Science and Engineering Library are marked R.)
- PSpice™ is available by download from Orcad or from the UTA HKN chapter.
- Prof. Dillon’s excellent tutorial for PSpice™ is at http://rock.uta.edu/dillon/pspice/

Cadence References:
- UTA Cadence™ website
- Cadence Helps at http://www.uta.edu/ronc/4345sp02/cadence

Grading Scale:
- A = 90 and above
- B = 75 to 89
- C = 60 to 74
- D = 50 to 59
- F = 49 and below
Problems: The problem assignments shown in the syllabus have been selected for your study, but will not be collected or graded. The study of the problems assigned will be helpful in preparing for the tests and final.

Grade Calculation: Each team participant will receive a grade on each project report based on team performance (including inputs from the other teams) and individual performance (including inputs from the team members). The grade will be the average of the four project assignment grades and the final exam. The individual weighting is still tbd.

Grading Formula:
- 30% total, 2 Team Reports for 15% each
- 20%, Team Design Project
- 20% Individual Design Project
- 15% Test 1 see http://www.uta.edu/ronc/4345sp02/Test01Sp02HelpSheet.pdf
- 15% for final (required) see http://www.uta.edu/ronc/4345sp02/FinalSp02HelpSheet.pdf

Project Assignments:

For Individual and Group Design Projects, go to http://www.uta.edu/ronc/4345sp02/projects

Team Reports – the class will form into teams of 4 to 6 to do 5 project assignments. The teams will organize themselves and propose their own business plan and structure. Once the team organization is approved, the team will continue as formed throughout the entire course.

1. Technology: RFPs (requests for proposals) will be published calling for rank order bids for development of the Technology Presentations (TPs). Each team will be assigned a TP based on the best proposals for each RFP. The team will make a class presentation for the TP as shown on the syllabus. Note Chapter listings are from the text - if a section is listed, that includes all subsections.
   1.1 Chapter 2 - 2.1 to 2.4
   1.2 Chapter 2 - 2.5 through 2.7
   1.3 Chapter 3 - Ch 3 - 3.1
   1.4 Chapter 3 - 3.2
   1.5 Chapter 3 - 3.3
   1.6 Chapter 4 - Ch 4 - 4.1 through 4.3.1
   1.7 Chapter 4 - 4.3.2(except CMOS and BiCMOS) through 4.4.2
   1.8 Chapter 5 - Ch 5 - 5.1 through 5.4
   1.9 Chapter 5 - 5.5 through 5.6
   1.10 Chapter 6 - Ch 6 (all)
   1.11 Chapter 7 - 7.1 through 7.2.6
   1.12 Chapter 7 - 7.2.7 through 7.3.2

2. Design: As #1 above, applied to the Design Presentations (DPs). [Note: ADAIC refers to sections in Analysis and design of analog integrated circuits, 4th ed. Emphasis should be placed on BJT material. If a section is listed, that includes all subsections]
   2.1 Chapter 8 - 8.1
   2.2 Chapter 8 - 8.2
   2.3 Chapter 8 - 8.3
   2.4 Chapter 9 - 9.1
   2.5 Chapter 9 - 9.2 and 9.3
   2.6 Chapter 10
   2.7 ADAIC 4.1 through 4.3
   2.8 ADAIC 4.4 through A.4.2
   2.9 ADAIC 5.1 through 5.2, and 5.4
   2.10 ADAIC 6.8 and 6.9
   2.11 ADAIC 7.1 through 7.2
   2.12 ADAIC 7.3 through 7.5

06/20/02, 3:38 PM Version
3. Product Design: A linear bipolar integrated circuit product will be defined for the class Product Design Project. Each team will develop a complete design for processing at the MOSIS (http://www.mosis.com) foundry. The development tools available are in Cadence (http://www.cadence.com).


First Assignment:
1. Each student should immediately send e-mail to ronc@uta.edu with a line including the e-mail address(es) to which you want class communications sent.
2. Interact with fellow class members to begin to form project groups of 4 to 6. Group formation proposals will be due 02/22/02.
3. Frequently refresh your web browser at http://www.uta.edu/ronc/4345sp02/ for complete class data.

Student Evaluation of Teaching: Students will complete evaluation forms at the end of the semester.
Lecture, Assignment, Quiz and Test Schedule
(When published, lecture notes will be at http://www.uta.edu/ronc/4345sp02/lectures/)

<table>
<thead>
<tr>
<th>CL</th>
<th>DATE</th>
<th>DAY</th>
<th>STUDY ASSIGNMENTS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>15-Jan-01</td>
<td>T</td>
<td>Ch 1 - Device Physics (daily lectures at link above)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>17-Jan-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>22-Jan-01</td>
<td>T</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>24-Jan-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>29-Jan-01</td>
<td>T</td>
<td>Unix environment and Cadence Tools - NH 242</td>
<td>Jan 30</td>
</tr>
<tr>
<td>6</td>
<td>31-Jan-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>05-Feb-01</td>
<td>T</td>
<td>Cadence Tools - NH 242</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>07-Feb-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>12-Feb-01</td>
<td>T</td>
<td>Ch 2 - Semiconductor Fabrication (TP 1.1 and 1.2)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>14-Feb-01</td>
<td>Th</td>
<td>Ch 3 - Representative Processes (TP 1.3 and 1.4)</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>19-Feb-01</td>
<td>T</td>
<td>Ch 3(cont.) and Ch 4 - Failure Mechanisms (TP 1.5 and 1.6)</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>21-Feb-01</td>
<td>Th</td>
<td>Ch 4(cont.) and Ch 5 - Resistors (TP 1.7 and 1.8)</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>26-Feb-01</td>
<td>T</td>
<td>Ch 5(cont.) and Ch 6 - Capacitors (TP 1.9 and 1.10)</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>28-Feb-01</td>
<td>Th</td>
<td>Ch 7 - Matching of Resistors and Capacitors (TP 1.11 and 1.12)</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>05-Mar-01</td>
<td>T</td>
<td>Ch 8 - Bipolar Transistors (DP 2.1 and 2.2)</td>
<td>Mid-Term Mar 08</td>
</tr>
<tr>
<td>16</td>
<td>07-Mar-01</td>
<td>Th</td>
<td>Ch 8(cont.) and Ch 9 - Applications of BJTs (DP 2.3 and 2.4)</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>12-Mar-01</td>
<td>T</td>
<td>Project work day</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>14-Mar-01</td>
<td>Th</td>
<td>Test 1*</td>
<td>Spring Vac. 3/18 to</td>
</tr>
<tr>
<td>19</td>
<td>26-Mar-01</td>
<td>T</td>
<td>Ch 9(cont.) and Ch 10 - Diodes (DP 2.5 and 2.6)</td>
<td>3/18 to</td>
</tr>
<tr>
<td>20</td>
<td>28-Mar-01</td>
<td>Th</td>
<td>Current Mirrors, Active Loads, and References (DP 2.7 and 2.8)</td>
<td>Easter Hol. 3/29 to</td>
</tr>
<tr>
<td>21</td>
<td>02-Apr-01</td>
<td>T</td>
<td>Output Stages and Op-Amps (DP 2.9 and 2.10)</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>04-Apr-01</td>
<td>Th</td>
<td>Frequency Response of Integrated Circuits (DP 2.8 and 2.12)</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>09-Apr-01</td>
<td>T</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>11-Apr-01</td>
<td>Th</td>
<td></td>
<td>Last drop on 4/16</td>
</tr>
<tr>
<td>25</td>
<td>16-Apr-01</td>
<td>T</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>18-Apr-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>23-Apr-01</td>
<td>T</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>25-Apr-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>30-Apr-01</td>
<td>T</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>02-May-01</td>
<td>Th</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>09-May-01</td>
<td>Th</td>
<td>Final - 11:00 AM to 1:30 PM - Grades due 5/14 (Summer sem. begins 5/2)</td>
<td></td>
</tr>
</tbody>
</table>

* Click [http://www.uta.edu/ronc/4345sp02/Test01Sp02HelpSheet.pdf](http://www.uta.edu/ronc/4345sp02/Test01Sp02HelpSheet.pdf) to download a Help Sheet for use on Test 1

Notes:
1. This syllabus may be changed by the instructor as needed for good academic practice.
2. Quizzes and tests are open book (must have a legally obtained copy—no Xerox copies). Calculator allowed.
3. There will be no make-up, or early exams given. Attendance is required for all tests.
4. Americans with Disabilities Act: The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 93112—The Rehabilitation Act of 1973 as amended. With the passage of new federal legislation entitled Americans with Disabilities Act – (ADA), pursuant to section 504 of The Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens. As a faculty member, I am required by law to provide “reasonable accommodation” to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with informing faculty at the beginning of the semester and in providing authorized documentation through designated administrative channels. In conformance with the Americans with disabilities Act, I state that, “If you require an accommodation based on disability, I would like to meet with you in the privacy of my office during the first week of the semester to make sure you are properly accommodated. Contact Mr. Jim Hayes (272-3364) for Information.”
5. It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University. “Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts.” (Regents' Rules and Regulations, Part One, Chapter VI, Section 3, Subsection 3.2, Subdivision 3.22). ANY CHEATING WILL RESULT IN SEVERE PENALTIES. All work submitted must be original. If derived from another source, a full bibliographical citation must be given.
6. If identical papers are submitted by different students, the grade earned will be divided among all identical papers.
7. A paper submitted for regrading will be compared to a copy of the original paper. If changed, points will be deducted.