EE5343 – Silicon Integrated Circuit Fabrication Technology
Spring 2012
Course Syllabus

Instructor: Prof. SAMIR IQBAL

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Office Hours: TTh 2:45 – 3:45 pm

Section Information:

Section 001: Lecture
Room and Time: NH 229, Tuesdays and Thursdays, 12:30-1:50 PM
Section 101: Lab
Room and Time: NANO 104, Wednesdays, 9 AM-12:50 PM
Section 102: Lab
Room and Time: NANO 104, Fridays, 9 AM-12:50 PM

Course GTA: TBD
Course GTA O/Hs: TBD

Prerequisite:

Attend the NanoFAB Safety and Cleanroom training and pass the quiz.

Required Textbook and Other Course Materials:

Introduction to Microelectronic Fabrication, Modular Series on Solid State Devices Vol. V, Second Edition, by Richard C. Jaeger, Prentice-Hall, 2002. ISBN 0-201-44494-7

Reference Textbook:

Silicon Processing for the VLSI Era, Volume 1 - Process Technology, Second Edition, by: S. Wolf and R. N. Tauber. ISBN: 0-9616721-4-5. http://www.latticepress.com/vol1page2.html

Description of Course Content:

Course comprises of lectures and labs. Introduction to the basic steps and processes of fabricating integrated circuit semiconductor devices: crystal growth (thin film and bulk), thermal oxidation, dopant diffusion/implantation, thin film deposition/etching, and lithography. Introduction to process simulators, such as SUPREM. Fabrication and characterization of resistors, MOS capacitors, junction diodes and MOSFET devices. Specifically we will cover:

1- Semiconductors and Insulators: Definition, crystal structures, physical properties.

2- Wafer Fabrication: Czochralski (CZ), Float Zone (FZ), Molecular Beam Epitaxy

3- Crystal Defects: Monovacancy, Divacancy, Microvoids, Voids, Antisites, Interstitials, Dislocation, Stacking fault, Grain Boundaries, Precipitates.

4- Diffusion:
a) Fick's first and second law and their solutions
b) Mechanism of diffusion
c) Profile and Junction Depth and techniques of their determination

d) Effect of electric field on diffusion process
e) Impurity diffusion in IC fabrication (Boron, Phosphorus, Ar).
f) Principles of SUPREM process simulation
g) Diffusion Systems [equipment, sources (gas, liquid, solid)]
h) Measurement techniques.

5- Thermal Oxidation and Nitridation of Silicon
a) Oxidation kinetics (general solution, Parabolic and linear growth and empirical modifications to the growth rate of SiO_2 and its kinetics)
b) Thermal nitridation
c) Factors in oxidation
d) Applications of oxide and nitride layers in IC fabrication.
e) SiO_2/Si interface, charge traps and impurities redistribution at the interface.
f) Oxidation systems.
g) Measurement techniques

6- Ion Implantation:
a) Dose, Beam Current, Range and Projected Range
b) Projected and Lateral Straggle
c) Ion Stopping (nuclear and electronic energy loss mechanism)
d) Implantation in amorphous and single crystal (channeling effect)
e) Ion implantation damage
f) Electrical activation and implantation damage recovery (Annealing and RTP)
g) Ion Implantation equipment
h) Masking layers
i) Shallow Junction
j) Measurement techniques

7- Photolithography:
a) Photolithography steps (Coat, Soft bake, Patterning and Exposure, Post Exposure Bake, Develop, Inspection)
b) Photoresists (positive and negative)
c) Resist chemistry (Photo sensitive and base)
d) Physical properties (Sensitivity, Photo Speed, Resolution, etc.)
e) Coat and Coaters (Thickness control, uniformity, etc.)
f) Soft Bake and its effects on the film properties and consequent steps
g) Patterning and exposure, Criteria, limits, resist dependency, equipment, alignment, etc.)
h) Bosung Curves, Focus-exposure matrix
i) Post Exposure Bake, and its effects on the pattern
j) Develop (batch, spray, and puddle)
k) Developer chemistry, develop time
l) Critical Dimensions (CD) and Inspection (pattern integrity, notching, bridging, etc.)

8- Interconnects:
a) Metal (Al, Ti, TiN, W, etc.)
b) CVD and PVD techniques and systems,
c) Al, Al:Si, Al:Si:Cu in VLSI (properties, alloys, etc.)

d) Sputter Deposition for VSLI (glow discharge, RF sputter, magnetron sputter, mechanism, deposition rate, advantages and disadvantages, etc.)
e) Contacts and Vias
f) Morphology and Step Coverage, Aspect Ratio
g) Refractory Metals and applications
h) Barrier metals
i) Ohmic and Schottky contacts
j) Silicide formation
k) Effects of contamination (water, carbon, etc.)
l) Planarization and Passivation
m) Chemical Mechanical Polishing

9- Etch:
a) Etch type (wet, dry)
b) Dry Etch, Plasma etch (Process, mechanism, its chemistry and physics)
c) Reactive Ion Etching (Process, mechanism, characteristics. damage etc.)
d) Wet Etching (chemical and chemistry, etch rate, application and process, etc.)

10- Process Integration and Device Fabrication (all steps)

11- Cleanroom

12- Statistical Process Control, Charts, Limits, Determination of Limits, etc.

Requirements of Lab Work:

- Lab work will be done in Nanotechnology Research and Teaching Facility (NanoFAB), room 104.
- Every student has to attend the "NanoFAB Safety & Protocol Class" and pass the associated quiz.
- Every student has to undergo "General HAZCOM Online Training."
- The students who do not pass these trainings will be administratively dropped from the course.
- Details are given at following link on how to register for the trainings:
  http://www.uta.edu/engineering/nano/user.php
- **Until all required Training is completed, a student will not be given access to lab facilities, will not be able to participate in any lab activities, and will earn a grade of zero for any uncompleted work.**
- In the lab part of the course, the basics of each step of the process will be practiced. This includes oxidation, metallization, photolithography, etch, etc.
- Each student is assigned to a ~4 hour lab session every week. Be in the lab on time.
- Lab sections and times can not be changed, switched or altered.
- Students will use the available facilities to construct a capacitor with different oxide films (one oxide film will be processed at the UTA facility and two types will be provided to them from NSC) as their project. All capacitors will be tested.

Student Learning Outcomes:

The desired learning outcomes for student of this course are:

- Able to design integrated silicon based devices' process steps

- Understand all silicon fabrication processes, their metrologies and related theory
- Develop an understanding of the complexities involved in a complete fabrication cycle of an integrated circuit.
- Learn theory and practical techniques for optical lithography processes
- Gain the basic concept of FEOL/BEOL integration flow
- Describe the basic processes of FEOL
- Understand challenges of new materials and 3D CMOS devices for lithography
- Identify the challenges and interactions between lithography and all the critical processes
- Describe BEOL copper/low-k dual damascene integration schemes

To achieve these outcomes, the following learning objectives are established:

#	Course Learning Objective (CLO)	Assessment approach
1	Ability to design and analyze at least two-mask level silicon based device	Exam Problems
2	Ability to use equipment, process and chemical reactivity data to define a process flow for a particular fabrication module	Project Lab Notebook
3	Ability to differentiate and analyze basic trade-offs in processing parameters and how these affect the desired process output	Exam Problems
4	Knowledge of basic limitations of different processes and how these integrate to achieve final device	Homework/Exam Problems
5	Experimentally test and characterize the fabricated devices	Project Lab Notebook
6	Working knowledge of basic equations that govern the processes used in fabrication	Exam Problems
7	Understanding of fundamental challenges in fabrication techniques and possible solutions	Term Paper
8	Compare theory with experiments and identify sources of error and discrepancy	Homework Problems
9	Clarity in written communication to explain approaches and results, and to compare with expected results	Term Paper
10	Write critical report(s) on the fabrication process	Project Lab Notebook

Descriptions of Major Assignments and Examinations with Due Dates:

The course requires several homework assignments, one term paper, properly maintained lab notebook and two exams. Wikipedia and/or other websites can not be used as a reference in any of the assignments of this course. Most of the assignments/projects are to be submitted through the Blackboard (http://www.uta.edu/blackboard/). Name your file with your First and Last name followed by assignment name. For all assignments, present your original work. Each individual assignment has to be worked out by individual student. Look under “Academic Integrity” for further details.

Homework: Not more than once a week, a set of problems related to the current course material will be assigned. These will be generally due at the start of lecture after a week.

Term Paper: Towards the goals of developing a more interactive classroom environment and practicing analytical thinking and communication skills, each student has to write a term paper. The goal is to learn the process by which researchers, practicing engineers, and technology advisors, acquire, distill, process and present technically sound ideas based on alternative technological approaches to solve a problem. The aim is to turn data into meaningful information, and information into intelligence (actionable information).

The paper has to address a problem of **semiconductor fabrication and processing**. Breakdown the paper in three distinct sections. The first section, the abstract, should describe and define the new idea on one page. Second part should provide a synopsis of impeding problems/limitations that are addressed and analysis of the state of the art. The third and most important part of the paper should present a technically sound detailed solution backed with theory, data or simulation. The term paper will be due on March 20, 2012 (10^{th} week of the semester).

The one-page abstract of the paper will be shared with the rest of the class. Each student will be asked to talk ~10 minutes about the idea of the term paper. Everyone will be invited (and expected) to participate in the discussion.

The term paper should be normally on a topic not covered in the class. Restrict the paper to 6 pages (excluding cover page and references). Use Arial font size 11 or larger. The margins on top, bottom, left and right of the page should not be less than 1 inch. Proper referencing should be done using IEEE styling format given at following web address:

http://www.ieee.org/documents/ieeecitationref.pdf

Project Lab: The lab notebooks will be collected at least twice during the semester without prior announcement. The lab notebooks should have detailed records of all activities and experiments carried out in the lab under the headings of Objective, Procedure, Equipment and Supplies, Precautions, Observations, Diagrams. The lab notebook should have numbered pages. Include details like data, data plots, data analysis, figures, sketches, diagrams, micrographs, pictures, etc. to support your observations. The other factors in grading for project lab will include reports of the experiments and performance in the lab.

Exams: All exams will be closed books and will be conducted in NH229. Midterm exam will be on 01 March 2012 during class time. The final exam will be as per the schedule posted at the below link. It will be on May 10, 2012 between 11-1:30 pm.

http://wweb.uta.edu/ses/recordsandregistration/content/student_services/final_exam_schedule.aspx

Grading Policy:

The final grade will be calculated as per the following breakdown:

Homework:	10%
Term paper:	20%
Project Lab:	25%
Midterm Exam:	20%
Final Exam:	25%

Re-grade Request: If you are not satisfied with your grade on any assignment, report or exam, write down a “Re-grade Request” detailing why your grade should be modified. Turn in the actual graded assignment, report or exam with your “Re-grade Request.” A “Re-grade Request” can be turned in **within 7 days** from the day that the graded assignment, report or exam was given back to the student.

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Attendance Policy:

The course content will evolve around class-discussions and laboratory fabrication. It is important to attend the lecture and **essential** to be in the lab during the assigned days to grasp the concepts and follow the material. If you can not attend the lab session you are registered for, due to a valid reason, provide one week advance notice to the instructor and get approval. Be prepared to present documentation to support the need.

Make-up Exam/Assignment Policy:

If a student can not meet an assignment deadline or appear for an exam or presentation, give the instructor/GTA an advance notice. Email the instructor, call a friend to email the instructor or meet the instructor before any anticipated conflict of schedule. No credit will be given for the missed assignment unless such absence/delay/failure-to-deliver occurs due to a documented emergency. You may be asked to furnish further evidence to confirm the nature of emergency.

Drop policy:

The UTA drop policy will be adhered to. For a time table see links at

http://www.uta.edu/universitycollege/current/academic-planning/need-to-know-policies/schedule-changes.php

Students may drop or swap (adding and dropping a class concurrently) classes through self-service in MyMav from the beginning of the registration period through the late registration period. After the late registration period, students must see the academic advisor to drop a class or withdraw. Drops can continue through a point two-thirds of the way through the term or session. It is the student's responsibility to officially withdraw if they do not plan to attend after registering. **Students will not be automatically dropped for non-attendance**. Repayment of certain types of financial aid administered through the University may be required as the result of dropping classes or withdrawing. Contact the Financial Aid Office for more information.

Americans with Disabilities Act:

The University of Texas at Arlington is on record as being committed to both the spirit and letter of all federal equal opportunity legislation, including the *Americans with Disabilities Act (ADA)*. All instructors at UT Arlington are required by law to provide "reasonable accommodations" to students with disabilities, so as not to discriminate on the basis of that disability. Any student requiring an accommodation for this course must provide the instructor with official documentation in the form of a letter certified by the staff in the Office for Students with Disabilities, University Hall 102. Only those students who have officially documented a need for an accommodation will have their request honored. Information regarding diagnostic criteria and policies for obtaining disability-based academic accommodations can be found at www.uta.edu/disability or by calling the Office for Students with Disabilities at (817) 272-3364.

Academic Integrity:

It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University. According to the UT System Regents' Rule 50101, §2.2, "Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are

attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts."

You are required to carefully read and sign the form titled "STATEMENT ON ETHICS, PROFESSIONALISM, AND CONDUCT FOR ENGINEERING STUDENTS." If you need soft copy of this statement, email the instructor/GTAs.

For the first occurrence of academic dishonesty by a student, a zero grade will be given on the exam, report, assignment, or project, as the case may be. Second occurrence of academic dishonesty by the same student (individual or in a team) will result in automatic reduction of one grade letter in the final grade of the course. The Office of Student Judicial Affairs will be informed in writing of academic dishonesty cases.

Plagiarism has many shapes, but can be explained in a few examples under the scope of this course. It maybe presenting someone else's published words (and work) in a way that these words (and works) do not clearly show the source. Any text from someone else's work can not be used "verbatim" unless in double quotes and followed by a citation and appropriate credit. If in doubt, ask the instructor/GTA.

Student Support Services Available:

The University of Texas at Arlington provides a variety of resources and programs designed to help students develop academic skills, deal with personal situations, and better understand concepts and information related to their courses. These resources include tutoring, major-based learning centers, developmental education, advising and mentoring, personal counseling, and federally funded programs. For individualized referrals to resources for any reason, students may contact the Maverick Resource Hotline at 817-272-6107 or visit www.uta.edu/resources for more information.

E-Culture Policy:

The University of Texas at Arlington has adopted the University "MavMail" address as the sole official means of communication with students. MavMail is used to remind students of important deadlines, advertise events and activities, and permit the University to conduct official transactions exclusively by electronic means. For example, important information concerning registration, financial aid, payment of bills, and graduation are now sent to students through the MavMail system. All students are assigned a MavMail account. ***Students are responsible for checking their MavMail regularly.*** Information about activating and using MavMail is available at http://www.uta.edu/oit/email/. There is no additional charge to students for using this account, and it remains active even after they graduate from UT Arlington.

To obtain your NetID or for logon assistance, visit https://webapps.uta.edu/oit/selfservice/. If you are unable to resolve your issue from the Self-Service website, contact the Helpdesk at helpdesk@uta.edu.

The instructor/GTAs will send important course-related information to your MavMail e-mail address ONLY. Your email to the instructor/GTA should also come from MavMail email account. Your email message sent from non-UT-Arlington accounts may never reach the instructor/GTA. You will be responsible for any misplaced or misdirected email that is sent from non-UT-Arlington email address.

Grade Grievance Policy:

If you have any grievance regarding a grade, consult with the instructor/GTAs. Information about the UT-Arlington grievance policy is at http://www.uta.edu/gradcatalog/general_info#grievances

Final Review Week:

A period of five class days prior to the first day of final examinations will be designated as FINAL REVIEW WEEK. The purpose of this week is to allow sufficient time for students to prepare for final exams. During this week, there will be no schedule or required activities such as field trips, seminars, or performances; and no themes, research problems or exercises of similar scope that have a completion date during or following this week will be assigned unless specified in the class syllabus. During Final Review Week, no exams constituting 10% or more of the final grade will be given, except make-up tests and laboratory examinations. In addition, no portion of the final exam will be given during Final Review Week.