Capacitance-voltage characteristics of Si and Ge nanomembrane based flexible metal-oxide-semiconductor devices under bending conditions

Minkyu Cho,1,2,a) Jung-Hun Seo,1,a) Dong-Wook Park,1 Weidong Zhou,3 and Zhenqiang Ma1(b)
1Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Wisconsin 53706, USA
2Department of Mechanical Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, South Korea
3Department of Electrical Engineering, NanoFAB Center, University of Texas, Arlington, Texas 76019, USA

(Received 29 April 2016; accepted 21 May 2016; published online 8 June 2016)

Metal-oxide-semiconductor (MOS) device is the basic building block for field effect transistors (FET). The majority of thin-film transistors (TFTs) are FETs. When MOSFET are mechanically bent, the MOS structure will be inevitably subject to mechanical strain. In this paper, flexible MOS devices using single crystalline Silicon (Si) and Germanium (Ge) nanomembranes (NM) with SiO2, SiO, and Al2O3 dielectric layers are fabricated on a plastic substrate. The relationships between semiconductor nanomembranes and various oxide materials are carefully investigated under tensile/compressive strain. The flatband voltage, threshold voltage, and effective charge density in various MOS combinations revealed that Si NM—SiO2 configuration shows the best interface charge behavior, while Ge NM—Al2O3 shows the worst. This investigation of flexible MOS devices can help us understand the impact of charges in the active region of the flexible TFTs and capacitance changes under the tensile/compressive strains on the change in electrical characteristics in flexible NM based TFTs. Published by AIP Publishing. [http://dx.doi.org/10.1063/1.4953458]
Flexible Si NM MOS devices show typical p-type MOS characteristics with clear accumulation and inversion regions. The inversion layer capacitance is defined by \[ C_{\text{inv}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{bulk}}}, \] where \( C_{\text{inv}} \) is the inversion layer capacitance, and \( C_{\text{bulk}} \) is the semiconductor capacitance. \( C_{\text{bulk}} \) depends on the depletion width in NMs. It should be noted that, when the NM is thin enough, the maximum depletion region may be limited by the thickness of NMs so that \( C_{\text{inv}} \) of Si NM MOS devices could be higher than \( C_{\text{inv}} \) of typical MOS capacitor on a bulk substrate.

Figures 2(a)–2(c) show the C–V characteristics of Si NM based flexible MOS devices with different dielectric materials (SiO2, SiO, and Al2O3) under different bending curvatures: concave molds with bending radii of 110.5 mm and 85 mm, and convex molds with bending radii of 77.5 mm, 38.5 mm, 28.5 mm, 21 mm, and 15.5 mm. It should be noted that, as shown in Figure S3, 1–V characteristics measured from reference metal-insulator-metal (MIM) structures with a SiO2, Al2O3, or SiO dielectric layer indicate sufficiently high breakdown electric field (\( E_F \)) with very low leakage current. The result agrees well with \( E_F \) values from other reports and confirms that the interface between the oxide and electrode does not affect the performance of flexible MOS capacitors. Raman frequency shifts are observed for NMs with different bending radii, as shown in Figure S1,22 and the corresponding strain values are calculated based on \[ \Delta \omega = -b_{\text{uni}} \times \nu_{\text{ox}}, \] where \( \Delta \omega \) is Raman frequency shift, \( b_{\text{uni}} \) is 337 for (100) Si in \((110)\) direction and 202 for (100) Ge in \((110)\) direction,8 is proportion constant, and \( \nu_{\text{ox}} \) is strain. For Si NMs, concave bending radii of 110.5 mm and 85 mm correspond to the compressive strain values, 0.16% and 0.32%, respectively, and convex bending radii of 77.5 mm, 38.5 mm, 28.5 mm, 21 mm, and 15.5 mm correspond to the tensile strain values, 0.16%, 0.32%, 0.48%, 0.63%, and 0.79%, respectively.

The flatband voltage (\( V_{\text{FB}} \)) for each strain condition was extracted using the corresponding flatband capacitance (\( C_{\text{FB}} \)) in the following equation and extracted from the measured C–V:7

\[ C_{\text{FB}} = \frac{C_{\text{max}}}{1 + \frac{(C_{\text{max}}/C_{\text{min}}) - 1}{2\sqrt{\ln(|N_A - N_D|/n_i)}}, \]

where \( C_{\text{max}} \) is the maximum capacitance, \( C_{\text{min}} \) is the minimum capacitance, \( N_A \) is the acceptor concentration, \( N_D \) is the donor concentration, and \( n_i \) is the intrinsic carrier concentration. As seen in Figure 2(d), \( V_{\text{FB}} \) shifts toward positive voltages as the applied strain increases. This phenomenon is clear in convex bending with tensile strain. The factors which affect the \( V_{\text{FB}} \) shift can be analyzed by the following equation:7

\[ V_{\text{FB}} = \phi_{\text{ms}} - \frac{Q_i}{C_{\text{ox}}}, \]

where \( \phi_{\text{ms}} \) is the metal-semiconductor work function difference, \( Q_i \) is the effective trap charge, which is the sum of effective oxide and interface charges \((Q_i = Q_{\text{ox}} + Q_{\text{it}}))\), and \( C_{\text{ox}} \) is the oxide capacitance. Based on Equation (2), the \( V_{\text{FB}} \) shift could be attributed to the change in effective trap charge or the change in the metal-semiconductor work function. The shift in \( V_{\text{FB}} \) is also related to the overall displacement of capacitance since \( V_{\text{FB}} \) is derived from \( C_{\text{FB}} \). So far, the \( V_{\text{FB}} \) shift in the MOS device under strain has been explained by the following reasons: gate metal work function shift, the dielectrostriction effect, or a combination of band-edge shift and the modulation of band-edge-to-Fermi-level separation.\(^9\)–11 Huang et al. and Choi et al. assumed that the strain-induced variation in interfacial trap charges and fixed oxide charges do not change appreciably under strain on rigid substrates.\(^10\)\(^,\)\(^11\) However, in addition to these factors, it is speculated that the \( V_{\text{FB}} \) shift in Si NM MOS devices can
be specifically attributed to the strain-induced change in trap charge density for several reasons. First, the uniaxial strain applied to NM MOS devices (up to 0.9%) is higher than the strain typically applied to rigid MOS devices. Thus, the strain-related factors could be more dominant. Second, higher fixed trap charges and interface charges may exist due to a poor silicon-oxide interface and a high defect density in the dielectric layer caused by the evaporation method. The high $C/V$ hysteresis shown in Figure S2 represents the high trap charge density in the evaporated dielectric layer. Although it is reported that thermal annealing could reduce the trap charge density for typical rigid MOS devices, the low melting temperature of the plastic substrates in flexible MOS devices hinders further high temperature annealing. Third, although we used the same anode metal for all devices, the different $V_{FB}$ shifts in strain in each oxide indicates dependencies on the types of oxide used in our flexible MOS devices, as shown in Figure 2(d). Figure 3 shows threshold voltage ($V_{th}$), effective charge ($Q_{eff}$), and effective charge density ($N_{eff}$) versus strain of SiNM MOS devices with different oxide materials, to compare the relationship between trap charge density and strain. In SiNM MOS devices, $V_{th}$ is increased as more tensile strain is applied to three types of devices: SiO$_2$ device (0.17 V/%), SiO device (0.29 V/%), and Al$_2$O$_3$ (0.12 V%). Both $Q_{eff}$ and $N_{eff}$ values are decreased as more tensile strain is applied: SiO$_2$ device ($-1.33 \times 10^{-8}$ C/, $-8.31 \times 10^{10}$ cm$^{-2}$/s), SiO device ($-2.09 \times 10^{-8}$ C/, $-1.30 \times 10^{11}$ cm$^{-2}$/s), and Al$_2$O$_3$ ($-5.29 \times 10^{-9}$ C/, $-3.30 \times 10^{10}$ cm$^{-2}$/s). Such decreases in...
$Q_{\text{eff}}$ and $N_{\text{eff}}$ values as more strain is applied could be related to increased electron trap density at the oxide/NM interface.

Figures 4(a)–4(c) show the C–V measurement results of flexible Ge NM MOS devices with different dielectric materials (SiO$_2$, SiO, and Al$_2$O$_3$) under various degrees of strain. For Ge NM, concave bending radii of 110.5 nm and 85 mm correspond to the compressive strain values, 0.37% and 0.19%, respectively, and convex bending radii of 77.5 mm, 38.5 mm, 28.5 mm, 21 mm, and 15.5 mm correspond to tensile strains, 0.19%, 0.37%, 0.56%, 0.75%, and 0.94%, respectively.

$V_{FB}$ is shifted in the positive direction for Ge NM MOS devices as more tensile strain is applied: SiO$_2$ device (0.11 V/%), SiO device (1.22 V/%), and Al$_2$O$_3$ device (2.01 V/%) (Figure 4(d)). This trend is similar to that of flexible Si NM MOS devices but more pronounced. Under the flat condition, C–V curves in Ge NM MOS devices are shifted in the positive direction compared to those of Si NM MOS devices due to different doping concentrations: Si NM ($1 \times 10^{15}$ cm$^{-3}$) and Ge NM ($1 \times 10^{16}$ cm$^{-3}$). The accumulation capacitances of Ge NM MOS devices are different from those of Si NM MOS devices even though both devices have the same oxide materials and thickness. This difference could be attributed to a poor material interface between the evaporated oxide layers and the Ge NM. Another noticeable difference between the C–V curves of the Ge NM MOS devices and the Si NM MOS devices is the inversion capacitance. Ge NM MOS devices show obscure inversion capacitance characteristics, and the inversion capacitance values are larger than those of Si NM MOS with the same types of oxide and thickness. This is because of the smaller Ge bandgap as well as the poor oxide-Ge NM interface. Therefore, evaporated oxide as a gate dielectric for Ge MOSFET with proper Ge surface passivation process is required.

$Q_{\text{eff}}$ and $N_{\text{eff}}$ values are comparable to those of Si NM MOS devices and show similar trends: SiO$_2$ device ($5.35 \times 10^8$ C/%, $3.029 \times 10^9$ cm$^{-2}$/%), SiO device ($5.39 \times 10^8$ C/%, $3.36 \times 10^{11}$ cm$^{-2}$/%), and Al$_2$O$_3$ device ($8.89 \times 10^8$ C/%, $5.55 \times 10^{11}$ cm$^{-2}$/%). In Ge NM MOS devices, the Al$_2$O$_3$ oxide layers were broken under tensile strain higher than 0.45% and we were unable to measure them further.

FIG. 4. C–V characteristics measured from Ge NM based flexible MOS devices under different bending conditions: (a) Au/SiO$_2$/Si NM; (b) Au/SiO/Si NM; (c) Au/Al$_2$O$_3$/Si NM; and (d) $\Delta V_{FB}$ ($V_{FB,bending} - V_{FB,nobending}$) versus strain.

FIG. 5. Calculated values of (a) threshold voltage ($V_{th}$), (b) effective charge ($Q_{\text{eff}}$), and (c) effective charge density ($N_{\text{eff}}$) under different bending conditions for Ge NM based flexible MOS devices.
In summary, single crystalline flexible MOS capacitors using Si NM and Ge NM were fabricated on plastic substrates, and the C-V characteristics were measured under various degrees of tensile/compressive strain. A high uniaxial strain (up to 0.94%) was applied to the MOS capacitors. The examination of flatband voltage, threshold voltage, and effective charge density in various combinations of dielectric materials and semiconductor materials revealed that the Si NM/SiO$_2$ shows the best interface charge behavior, while the Ge NM/Al$_2$O$_3$ structure shows the worst. The investigations of flexible MOS capacitors can help explain the change in the electrical characteristics of flexible TFTs that are fabricated using flexible single crystalline semiconductor NMs.

This work was supported from AFOSR PECASE under Grant No. FA9550-09-1-0482. The program manager is Dr. Gernot Pomrenke and by the BK21 plus program through the National Research Foundation (NRF) funded by the Ministry of Education of Korea.

22See supplementary material at http://dx.doi.org/10.1063/1.4953458 for the detailed strain analysis by Raman spectroscopy and breakdown electric field of dielectric layer.